# Offline Current Mode PWM Controller with BOP and Output OVP

## FEATURES

- Support DCM and CCM Operation
- ±1% CV Regulation
- Less than 75mW Standby Power
- Fixed 65KHz Switching Frequency
- Green Mode and Burst Mode Control
- Very Low Startup and Operation Current
- Built-in Frequency Shuffling to Reduce EMI
- Built-in Current Mode Control with Internal Slope Compensation
- Built-in Protections with Auto Recovery:
- VDD Under Voltage Lockout (UVLO)
- VDD Over Voltage Protection (OVP)
- Input Brownout Protection (Brownout)
- Output Over Voltage Protection (OVP)
- On-Chip Thermal Shutdown (OTP)
- Cycle-by-Cycle Current Limiting
- Over Load Protection (OLP)
- Leading Edge Blanking (LEB)
- CS Pin Float Protection

## APPLICATIONS

- Chargers and Adapter
- Motor Driver Power Supply

## GENERAL DESCRIPTION

DP2293 is a high performance current mode PWM controller for offline flyback converter applications. It supports DCM and CCM operation.

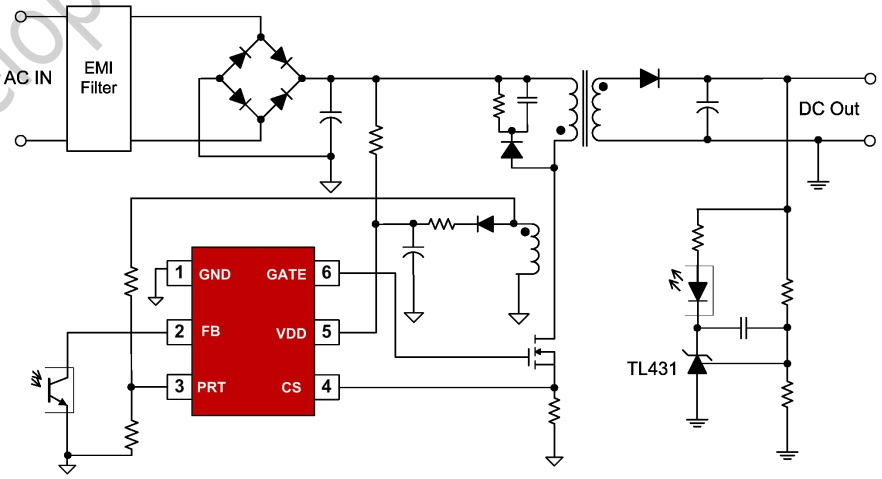
In DP2293, PWM switching frequency with shuffling is fixed to 65 KHz and is trimmed to tight range. The IC has built-in green and burst mode control for light and no load condition, which meet 6th energy star requirement and achieve less than 75mW standby power.

DP2293 integrates functions and protections of Under Voltage Lockout (UVLO), VDD over Voltage Protection (VDD OVP), Input Brownout Protection (Brownout), Programmable Output Over Voltage Protection (OVP), On-Chip Thermal Shutdown (OTP), Cycle-by-cycle Current Limiting (OCP), Over Load Protection (OLP), Soft Start, VDD clamping and CS Pin Float Protection, etc.。

## PACKAGE

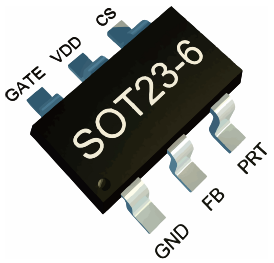
| Name | Description |
|---|---|
| DP2293 | SOT23-6,Halogen free,Reel,3000pc/reel |

## TYPICAL APPLICATION CIRCUIT



# PRODUCTS DESCRIPTION

## ➢ PIN CONFIGURATION




## ➢ PIN DISCRIPTION

| Pin | Name | I/O | Description |
|---|---|---|---|
| 1 | GND | P | The ground of the IC |
| 2 | FB | I | Feedback pin. The loop regulation is achieved by connecting a photo-coupler to this pin. PWM duty cycle is determined by FB voltage and the current sense signal at Pin 4 |
| 3 | PRT | I | Voltage sense for Brownout and OVP |
| 4 | CS | I | Current sense input pin |
| 5 | VDD | P | IC power supply pin |
| 6 | GATE | O | Totem-pole gate driver output to drive the external MOSFET |

## ➢ MARKING INFORMATION

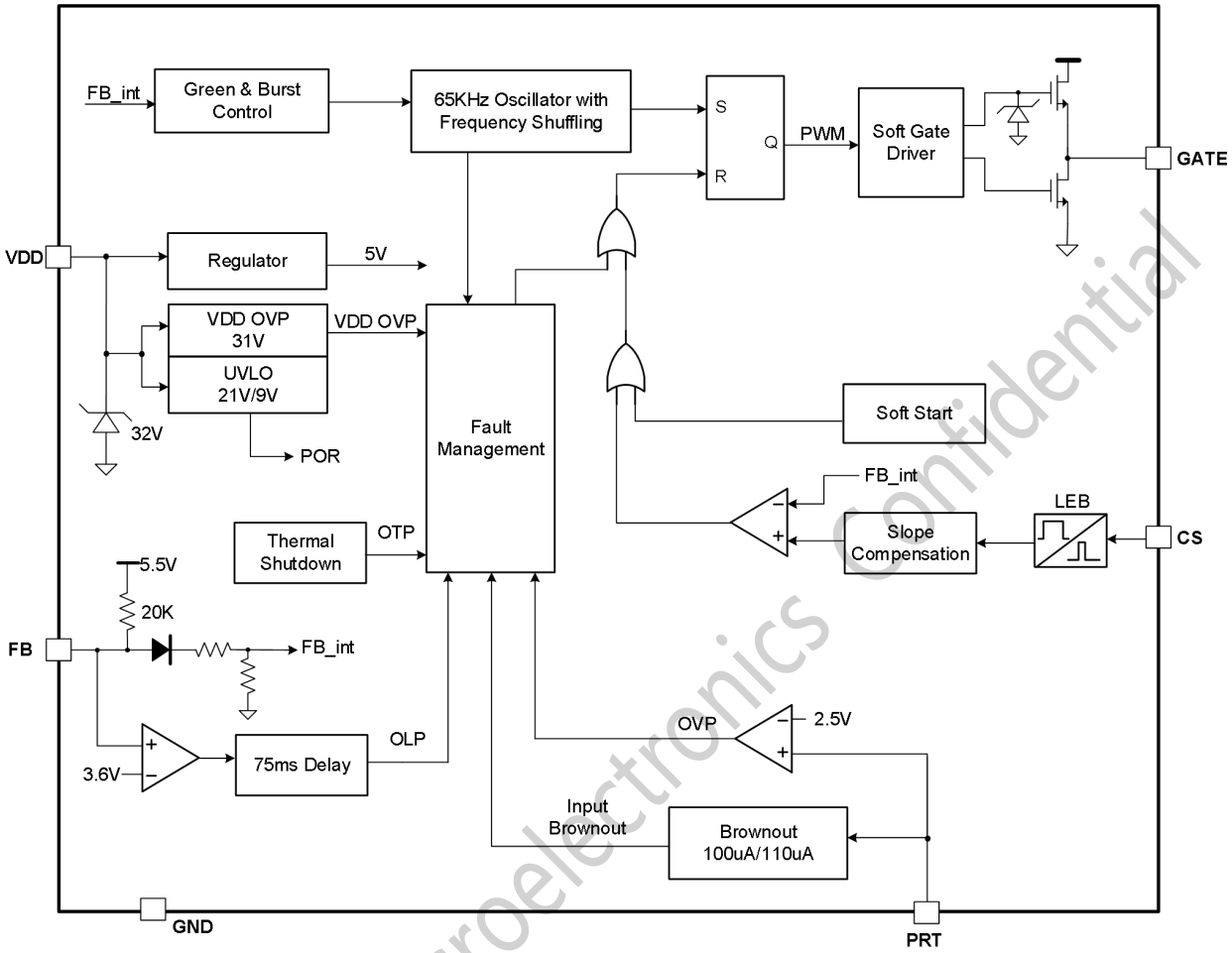

DPXX for product name;
DPXX is Product name; XXXX The first X represents the last year,2018 is 8; The second X represents the month, in A-L 12 letters;The third and fourth X on behalf of the date, 01-31 said;

## ➢ ABSOLUTE MAXIMUM RATINGS (NOTE 1)

| Parameter | Value | Unit |
|---|---|---|
| VDD DC Supply Voltage | 33 | V |
| VDD DC Clamp Current | 10 | mA |
| FB, CS, PRT voltage range | -0.3 to 7 | V |
| GATE voltage range | 20 | V |
| Package Thermal Resistance---Junction to Ambient (SOT23-6) | 250 | °C/W |
| Maximum Junction Temperature | 175 | °C |
| Storage Temperature Range | -65 to 150 | °C |
| Lead Temperature (Soldering, 10sec.) | 260 | °C |
| ESD Capability, HBM (Human Body Model) | 3 | kV |
| ESD Capability, MM (Machine Model) | 250 | V |

**Note1.**Stresses listed as the above "Maximum Ratings "may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to maximum rating conditions for extended periods may remain possibility to affect device reliability.

# BLOCK DIAGRAM



## RECOMMENDED OPERATION CONDITIONS (NOTE 2)

| Parameter | Value | Unit |
|---|---|---|
| Supply Voltage, VDD | 10 to 28 | V |
| Operating Ambient Temperature | -40 to 85 | °C |

## ELECTRICAL CHARACTERISTICS (TA=25℃, VDD=18V, unless otherwise noted)

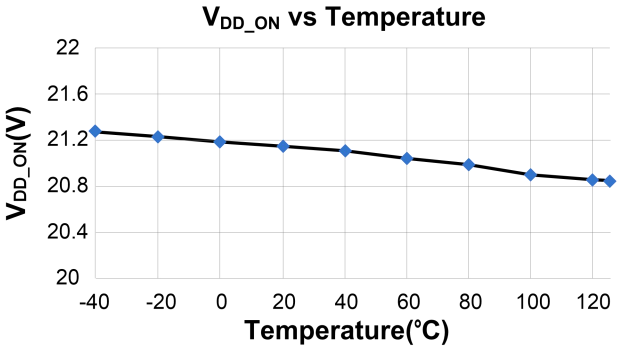
| Symbol | Parameter | Test Conditions | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| **Supply Voltage Section (VDD Pin)** | | | | | | |
| $I_{VDD\_st}$ | Start-up current into VDD pin | | | 2 | 20 | uA |
| $I_{VDD\_Op}$ | Operation Current | $V_{FB}$=3V, GATE=1nF | | 1.2 | 2 | mA |
| $I_{VDD\_standby}$ | Standby Current | | | 0.6 | 1 | mA |
| $V_{DD\_ON}$ | VDD Under Voltage Lockout Exit | | 19 | 21 | 21.5 | V |
| $V_{DD\_OFF}$ | VDD Under Voltage Lockout Enter | | 8 | 9 | 10 | V |
| $V_{DD\_OVP}$ | VDD OVP Threshold | | 29 | 31 | 33 | V |
| $V_{DD\_Clamp}$ | VDD Zener Clamp Voltage | $I(V_{DD})$ = 7 mA | 33 | 35 | 37 | V |
| **Feedback Input Section (FB Pin)** | | | | | | |
| $V_{FB\_Open}$ | FB Open Voltage | | | 5.5 | | V |
| $I_{FB\_Short}$ | FB Short Circuit Current | Short FB Pin to GND, Measure Current | | 0.3 | | mA |
| $Z_{FB\_IN}$ | FB Input Impedance | | | 20 | | KΩ |
| $A_{CS}$ | PWM Gain | $\Delta V_{FB}/\Delta V_{CS}$ | | 2.0 | | V/V |
| $V_{skip}$ | FB Under Voltage GATE Clock is OFF | | | 1.0 | | V |
| $V_{TH\_OLP}$ | Power Limiting FB Threshold Voltage | | | 3.6 | | V |
| $T_{D\_OLP}$ | Power Limiting Debounce Time | | | 75 | | ms |
| **Current Sense Input Section (CS Pin)** | | | | | | |
| $T_{LEB}$ | CS Input Leading Edge Blanking Time | | | 250 | | ns |
| $V_{cs\_max}$ | Cycle-by-cycle Current limiting threshold | | 0.97 | 1.0 | 1.03 | V |

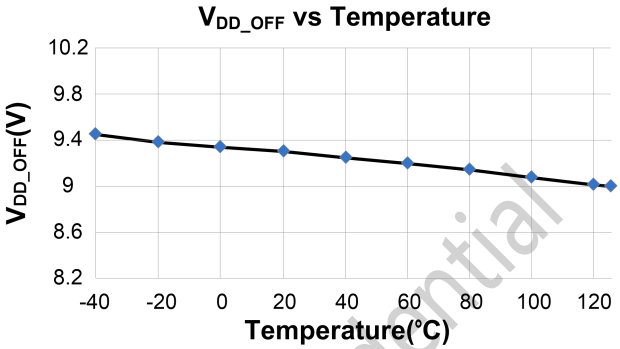
| | | | | | | |
|---|---|---|---|---|---|---|
| $T_{D\_OC}$ | Over Current Detection and Control Delay | GATE=1nF | | 70 | | ns |
| **Oscillator Section** | | | | | | |
| $F_{OSC}$ | Normal Oscillation Frequency | | 60 | 65 | 70 | KHz |
| $\Delta F(shuffle)/F_{OSC}$ | Frequency Shuffling Range | | -4 | | 4 | % |
| T(shuffle) | Frequency Shuffling Period | | | 32 | | ms |
| $D_{MAX}$ | Maximum Switching Duty Cycle | | | 66.7 | | % |
| $F_{Bust}$ | Burst Mode Base Frequency | | | 22 | | KHz |
| **Brownout and OVP Section (PRT Pin)** | | | | | | |
| $V_{OVP}$ | Over Voltage Protection Threshold | | | 2.5 | | V |
| $I_{Brownout\_Tr}$ | Brownout Trigger Current | | | 100 | | uA |
| $I_{Brownout\_Re}$ | Brownout Recovery Current | | | 110 | | uA |
| **On-Chip Thermal Shutdown** | | | | | | |
| $T_{SD}$ | Thermal Shutdown | (Note 3) | | 165 | | °C |
| $T_{RC}$ | Thermal Recovery | (Note 3) | | 140 | | °C |
| **DriverSection (GATE Pin) (Note 3)** | | | | | | |
| $V_{OL}$ | Output Low Level | Igate_sink=20mA | | | 1 | V |
| $V_{OH}$ | Output High Level | Igate_source=20mA | 7.5 | | | V |
| $V_{G\_Clamp}$ | Output Clamp Voltage Level | VDD=24V | | 13 | | V |
| T_r | Output Rising Time | GATE=1nF | | 150 | | ns |
| T_f | Output Falling Time | GATE=1nF | | 60 | | ns |

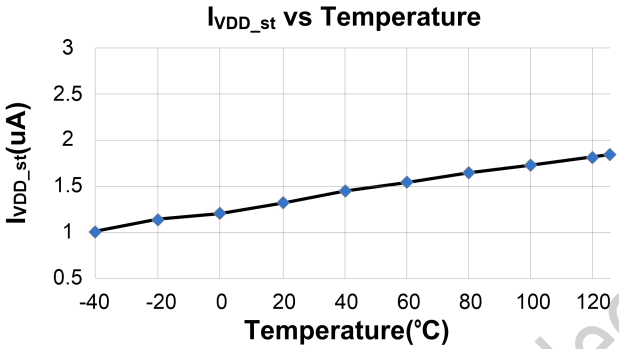
**Note2.** The device is not guaranteed to function outside its operating conditions.

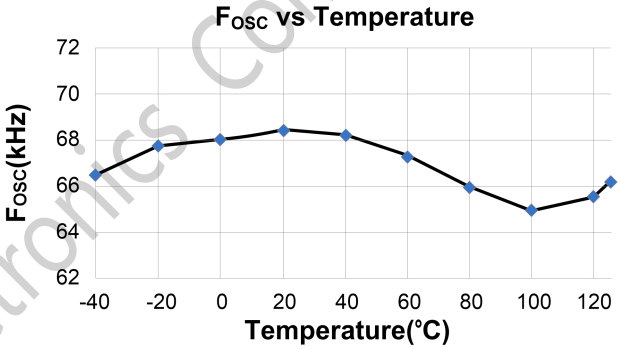
**Note3.** Guaranteed by the Design.

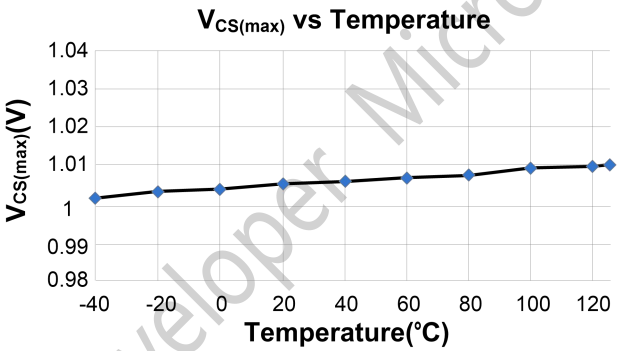
# CHARACTERIZATION PLOTS



# OPERATION DESCRIPTION

DP2293 is a high performance current mode PWM controller for offline flyback charger, motor driver power supply and adapter applications. The IC can support CCM and DCM operation, which is suitable for isolated power supply design that requires CV regulation of the output.

- **System Start-Up Operation and IC Operation Current**

Before the IC starts to work, it consumes only startup current (typically 2uA) which allows a large value startup resistor to be used to minimize the power loss and the current flowing through the startup resistor charges the VDD hold-up capacitor from the high voltage DC bus. When VDD reaches turn on threshold $V_{DD\_ON}$ (typical 21V), DP2293 begins switching and the IC operation current is increased to be 1.2mA (typical). The hold-up capacitor continues to supply VDD before the auxiliary winding of the transformer takes the control of VDD voltage.

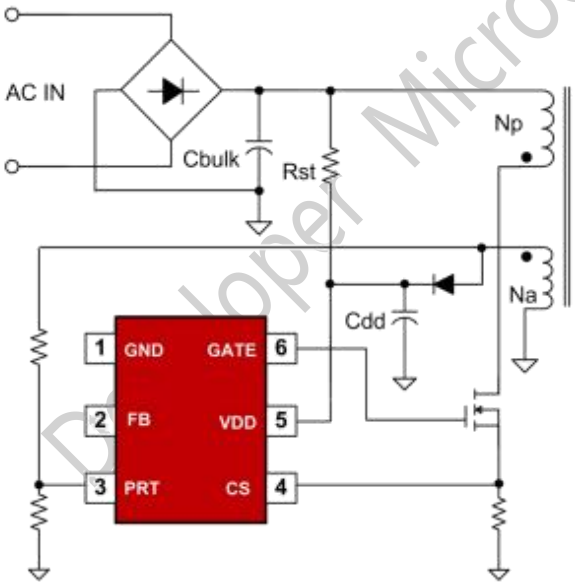



Fig.1

- **Oscillator with Frequency Shuffling**

PWM switching frequency in DP2293 is fixed to 65KHz and is trimmed to tight range. To improve system EMI performance, DP2293 operates the system with 4% frequency shuffling around setting frequency.

- **Green Mode Operation**

Since the main power dissipation at light/zero load in a switching mode power supply is from the switching loss which is proportional to the PWM switching frequency. To meet green mode requirement, it is necessary to reduce the switching cycles under such conditions either by skipping some switching pulses or by reducing the switching frequency.

- **Smooth Frequency Foldback**

In DP2293, a Proprietary "Smooth Frequency Foldback" function is integrated to foldback the PWM switching frequency when the loading is light. Compared to the other frequency reduction implementations, this technique can reduce the PWM frequency smoothly without audible noise.

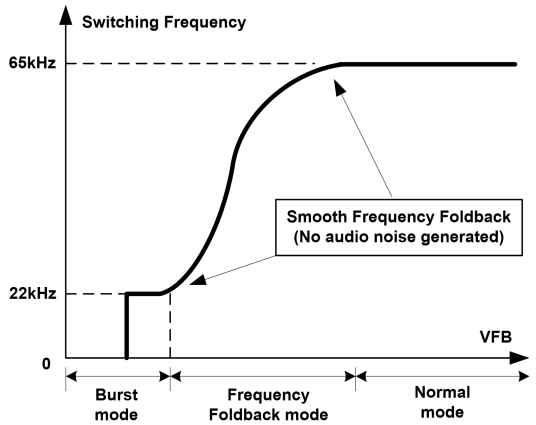



Fig.2

- **Burst Mode Control**

When the loading is very small, the system enters burst mode. When VFB drops below Vskip,

DP2293 will stop switching and output voltage starts to drop (as shown in Fig.3), which causes the VFB to rise. Once VFB rises above Vskip, switching resumes. Burst mode control alternately enables and disables switching, thereby reducing switching loss in standby mode.

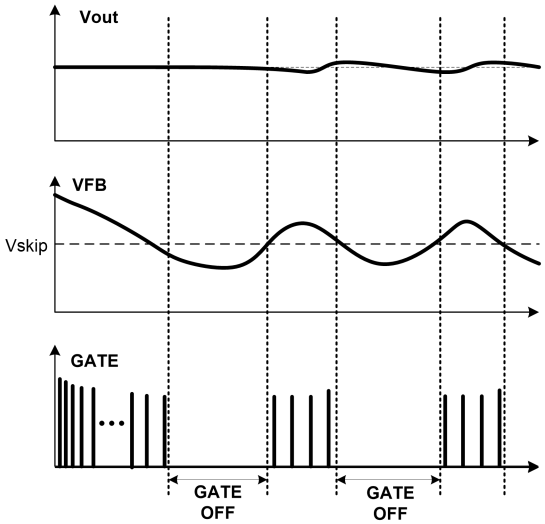



Fig.3

- **Built-in Slope Compensation**

In the conventional application, the problem of the stability is a critical issue for current mode controlling, when it operates in higher than 50% of the duty-cycle. In DP2293 the slope compensation circuit is integrated by adding voltage ramp onto the current sense input voltage for PWM generation. This greatly improves the close loop stability at CCM and prevents the sub-harmonic oscillation and thus reduces the output ripple voltage.

- **Leading Edge Blanking (LEB)**

Each time the power MOSFET is switched on, a turn-on spike occurs across the sensing resistor. The spike is caused by primary side capacitance and secondary side rectifier reverse recovery. To avoid premature termination of the switching pulse, an internal leading-edge blanking circuit is built in. During this blanking period (300ns, typical), the PWM comparator is disabled and cannot switch off the gate driver.

- **On Chip Thermal Shutdown (OTP)**

When the IC temperature is over 165°C, the IC shuts down. Only when the IC temperature drops to 140°C, IC will restart.

- **Soft Start**

DP2293 features an internal 2ms (typical) soft start that slowly increases the threshold of cycle-by-cycle current limiting comparator during startup sequence. It helps to prevent transformer saturation and reduce the stress on the secondary diode during startup. Every restart attempt is followed by a soft start activation.

- **Constant Power Limiting**

A proprietary "Constant Power Limiting" block is integrated to achieve constant maximum output power capability over universal AC input range. Based on the duty cycle information, the IC generates OCP threshold according to a proprietary analog algorithm.

- **Over Load Protection (OLP)**

If over load occurs and $V_{FB}$ is higher than $V_{TH\_OLP}$ for more than 75ms (typical), OLP protection will be triggered. The IC will experience an auto-recovery mode protection as mentioned above. The 75ms delay time is to prevent the false trigger from the power-on and turn-off transient.

- **VDD Over Voltage Protection (OVP) and Zener Clamp**

When VDD voltage is higher than 31V (typical), the IC will stop switching. This will cause VDD fall to be lower than $V_{DD\_OFF}$ (typical 9V) and then the system will restart up again. An internal 35V (typical) zener clamp is integrated to prevent the

IC from damage.

- **Output Over Voltage Protection (OVP) and Input Brownout Protection (BOP)**

DP2293 integrates programmable output over voltage protection (OVP) and input brownout protection (BOP). When the switching is off, the output voltage is sensed by the resistance divider across the auxiliary winding on PRT pin. If the voltage sensed on PRT pin is higher than $V_{OVP}$ (2.5V typical) last for 6 switching periods, the output over voltage protection (OVP) will be triggered. And the IC will stop switching and enter auto-recovery mode. When the switching is on, the voltage on PRT pin is clamped to low level. If the output current from PRT pin is less than $I_{Brownout\_Tr}$ (100uA typical), the input brownout protection (BOP) will be triggered. And the IC will also stop switching and enter auto-recovery mode. The IC will exit the BOP if the current is larger than $I_{Brownout\_Re}$ (110uA typical) dropped out from PRT pin.

- **CS Pin Float Protection**

When VDD voltage is higher than $V_{DD\_ON}$ (21V typical), IC firstly starts to check whether CS pin is floated. If CS pin is floated, switching is blocked and IC enters auto-recovery mode; otherwise, normal work begins. With this protection, system stability is enhanced.

- **Auto Recovery Mode Protection**

As shown in Fig.4, once a fault condition is detected, PWM switching will stop. This will cause VDD to fall because no power is delivered form the auxiliary winding. When VDD falls to $V_{DD\_OFF}$ (typical 9V), the protection is reset and the operating current reduces to the startup current, which causes VDD to rise. The system begins switching when VDD reaches to $V_{DD\_ON}$ (typical 21V). However, if the fault still exists, the system will experience the above mentioned process. If the fault has gone, the system resumes normal operation. In this manner, the auto restart can alternatively enable and disable the switching until the fault condition is disappeared.

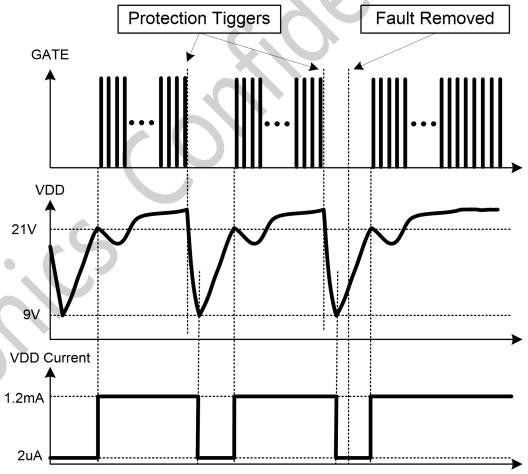


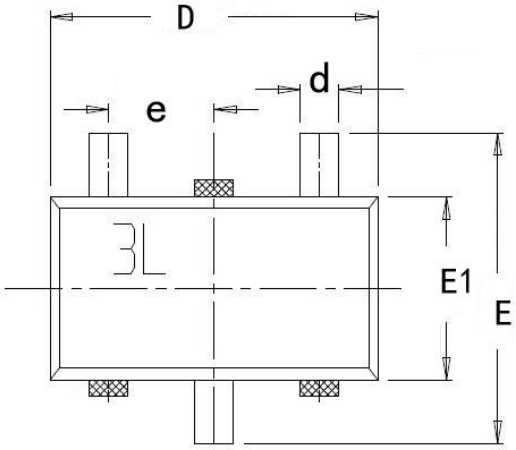

Fig.4

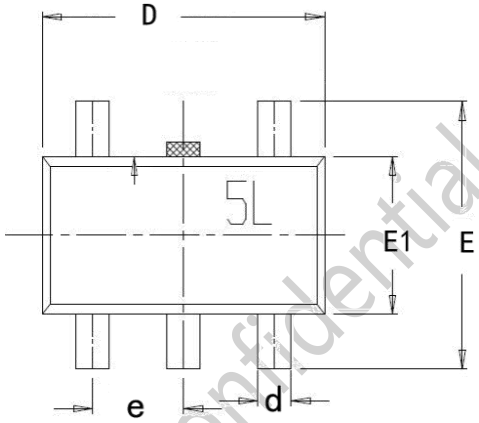
- **Soft Gate Driver**

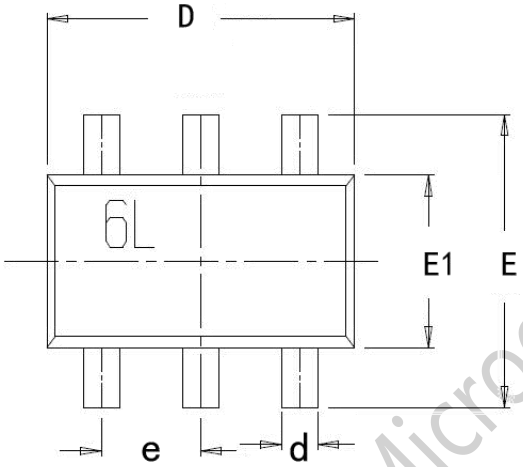
The output stage of DP2293 is a totem-pole gate driver with 400mA capability. Cross conduction has been avoided to minimize heat dissipation, increase efficiency, and enhance reliability. An internal 13V clamp is added for MOSFET gate protection at higher than expected VDD input. A soft driving waveform is implemented to minimize EMI.

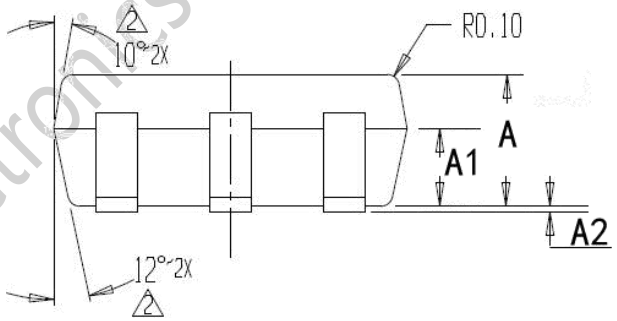
# PACKAGE DIMENSION

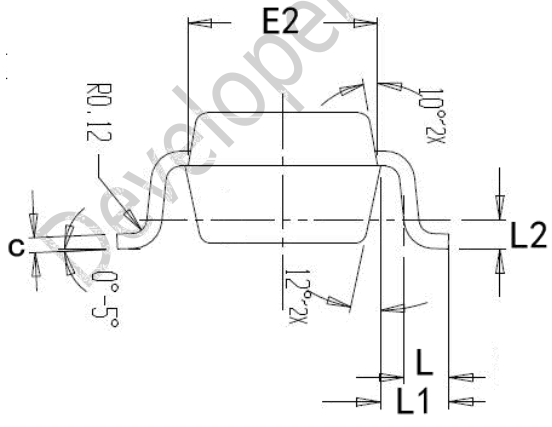
SOT23-6




| Symbol | Min | Nom | Max |
|---|---|---|---|
| A | 1.050 | 1.100 | 1.150 |
| A1 | 0.625 | 0.650 | 0.675 |
| A2 | 0.010 | 0.050 | 0.090 |
| c | 0.047 | 0.127 | 0.207 |
| D | 2.900 | 2.950 | 3.000 |
| d | 0.325 | 0.350 | 0.375 |
| E | 2.720 | 2.800 | 2.880 |
| E1 | 1.600 | 1.650 | 1.700 |
| E2 | 1.550 | 1.600 | 1.650 |
| e | 0.925 | 0.950 | 0.975 |
| L | 0.300 | 0.380 | 0.460 |
| L1 | 0.599REF | | |
| L2 | 0.250BSC | | |

# REVISION

| Editions | Revised Date | Redaction person | Revision content |
|---|---|---|---|
| REV1.0 | 2022/3/20 | AE | First edition |
| REV1.1 | 2024/9/14 | AE | Update Frequency |

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