DP3365S 16 Channel 64 scans Low-turning PWM Constant Current Driver

1 Overview

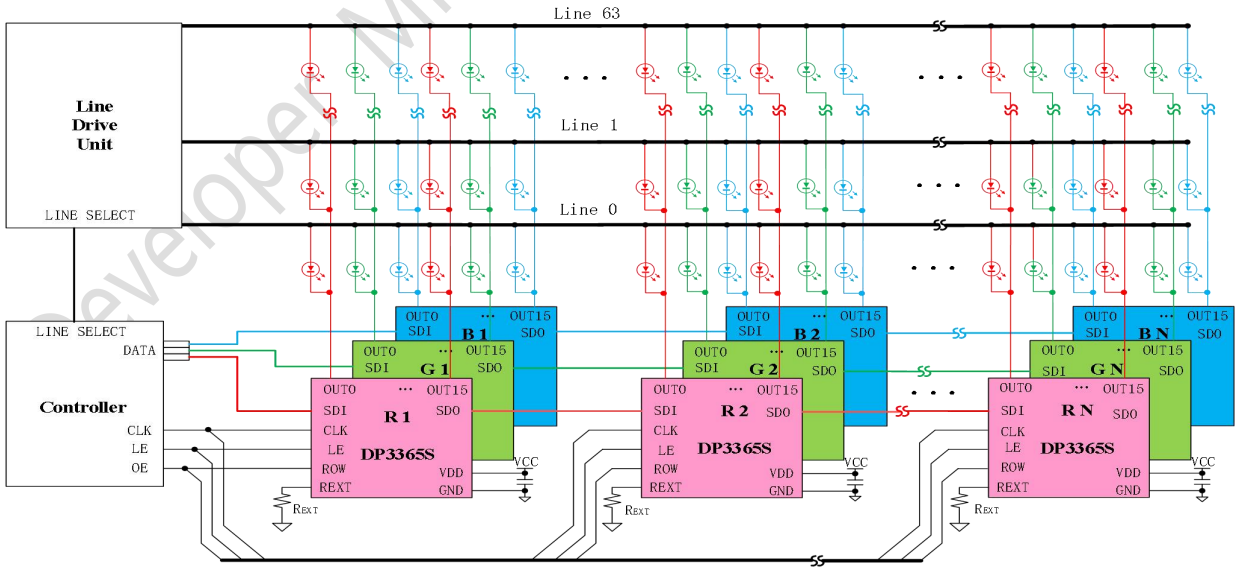
DP3365S is a common anode 16-channel low-turning PWM constant current driver chip designed for LED display, the chip supports a maximum of 16bit gray level, the chip integrates high-precision current generation circuit technology, so that the current error between the chips can be controlled within 2.0%, and integrates a variety of exclusive technology to improve the display effect of LED display. Can bring more improvement to the display.

2 Features

- Power supply voltage range：2.6～5.5V
- Operating temperature range：-40℃～85℃
- Scanned area：1 ~ 64 scans，arbitrarily adjustable
- 16 constant current output channels
- Support non-external resistor mode
- Constant current output range
  - 0.5mA～18mA （V_{out}=0.3V）
  - 0.5mA～25mA （V_{out}=0.6V）
- Inter-channel current error
  - Typical value：±1.2% Max：±2.0%
- Inter-chip current error
  - Typical value：±0.2% Max：±2.0%
- Supports up to 128x frame rate
- High gray independent refresh, no inter-frame black field
- Optimize the display effect
  - improve low gray uniformity
  - improve the first line darkening
  - improve up and down ghosting
  - improve high-low gray coupling
  - improve coupling of adjacent modules
- Internal Integration PLL produces internal GCLK with lower EMI
- Encapsulation mode：QSOP24/QFN24

3 Application Fields

- High refresh rate LED video display
- LED full-color display
- High density and small pitch LED panel display



DP3365S Typical Application Schematic

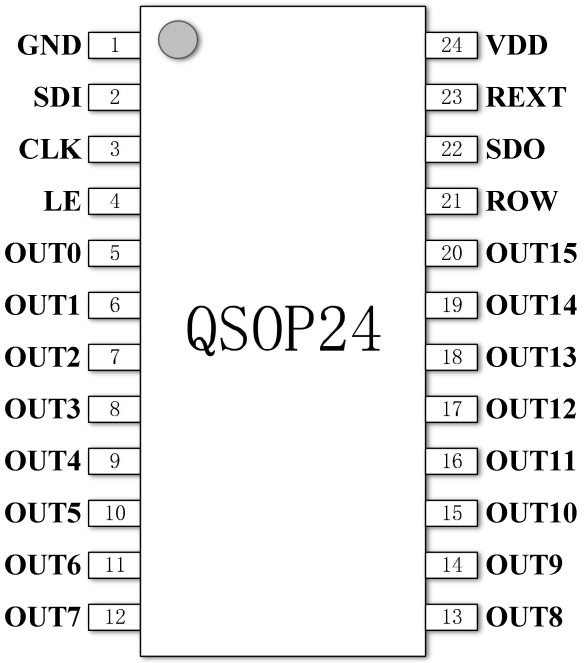
Content

Declaration

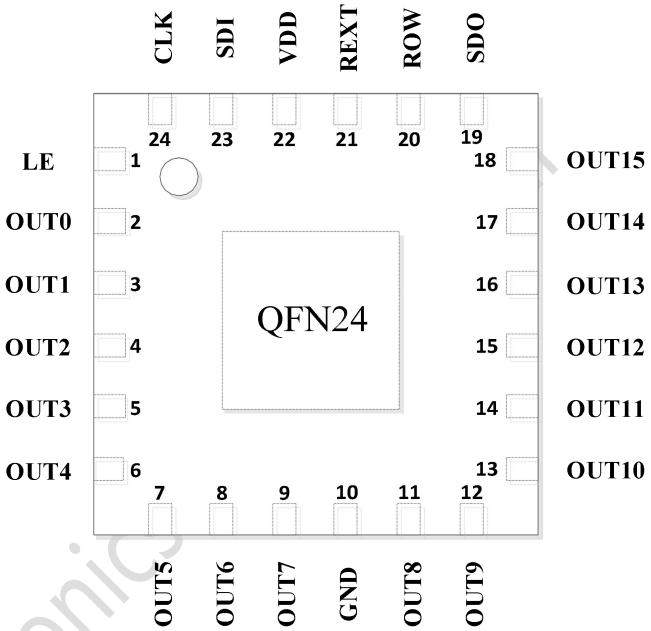
Version	Date	Reviser	Revised Contents
V1.0	2024.03	Wang Mei	Original Version
V1.1	2024.04	Wang Mei	1. Optimize the electrical parameters 2. Add the Non low inflection point diagram 3. Add the constant current accuracy test diagram

4 Products Description

- Pin Definition



QSOP24 Pin Definition Diagram



QFN24 Pin Definition Diagram

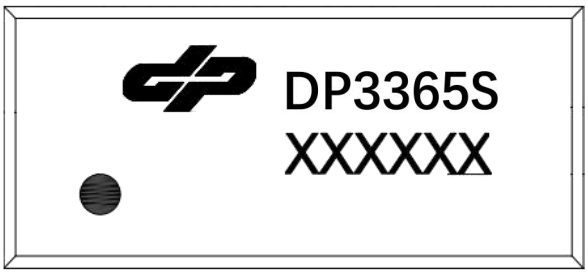
- Pin Description

QSOP24 Pin No.	QFN24 Pin NO.	Pin Name	Pin Description
1	22	GND	Chip Grounding Terminal
2	23	SDI	Serial Data Input Terminal
3	24	CLK	Serial Clock Input
4	1	LE	Data and Instruction Latch , different LE length represents different instructions
5 ~ 20	2 ~ 9 11 ~ 18	OUT0 ~ OUT15	Constant Current Output Terminal
21	20	ROW	Row Switching Signal
22	19	SDO	Serial Data Output
23	21	REXT	Connect the External Resistance Terminal
24	22	VDD	POWER END

- Product Purchase Information

Product Name	Encapsulation mode	Packing Method	Quantity/Disc	Humidity Level
DP3365S	QSOP24	Tape	4000	MSL=3
	QFN24	Tape	5000	

- Product Marking



QSOP24

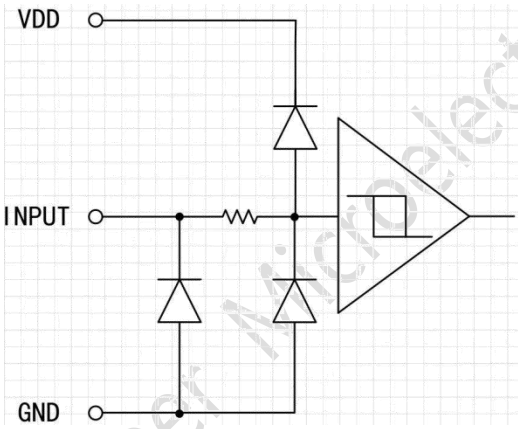
QFN24

DP3365S is the product name.
XXXXXX represents the product batch number.

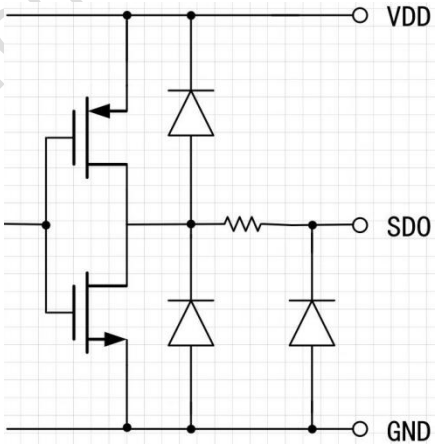
5 Electric schematic diagram

5.1 Input/Output Equivalent Circuit

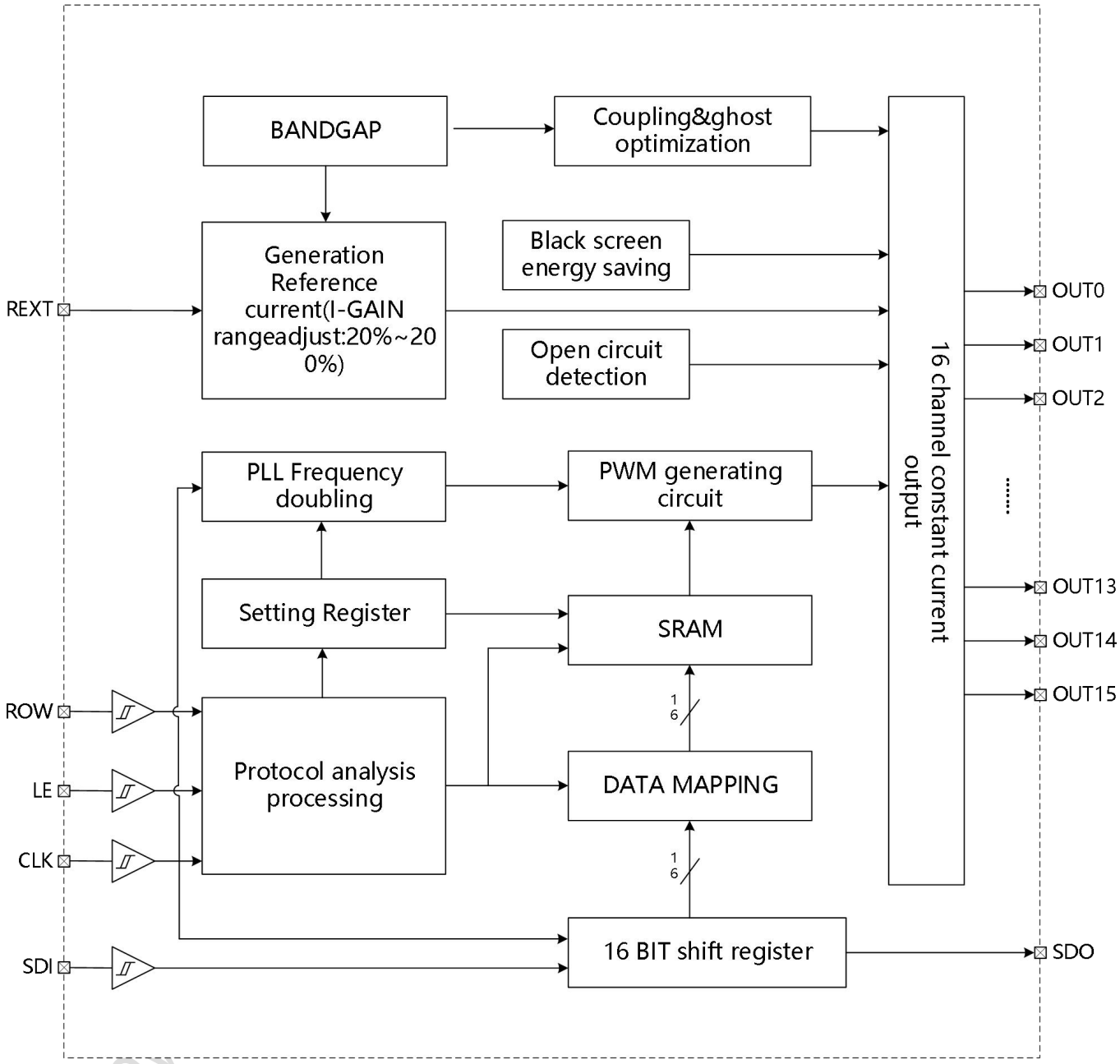
SDI,CLK,LE,OE Input terminal



SDO Output terminal



5.2 Internal Circuit Block Diagram



Internal circuit diagram

6 Parameter List

6.1 Maximum Limit Parameter

Project	Symbol	Rated Value	Unit
Supply Voltage	V_{DD}	0 ~ 6	V
Output Current	I_O	25	mA
Input Voltage	V_{IN}	-0.4 ~ V_{DD}+0.4	V
Output withstand voltage	V_{OUT}	11	V
Clock frequency	F_{CLK}	25	MHz
Operating Temperature	T_{opr}	-40 ~ 85	℃
Storage Temperature	T_{stg}	-55 ~ 150	℃

- All voltage values are based on the chip grounding terminal (GND) as a reference point, and the test temperature for the maximum limit parameter is 25℃.
- If the actual working conditions exceed the specified value may cause permanent damage to the components; If the actual operating conditions are slightly below the maximum and work for a long time, the reliability of the component may be reduced. The above values are only partially specified, and this product does not support functional operation under other conditions outside the specifications.
- The maximum peak welding temperature of surface paste products shall not exceed 260℃. The temperature curve shall be set by the factory according to J-STD-020 standard, the actual situation of the factory and the solder paste manufacturer's suggestion.

6.2 ESD Rating

6.2.1 Contact ESD

Symbol	Condition		Min Value	Typical Value	Max Value	Unit
$V_{(ESD)}$	Human-body model (HBM) [1]	OUTn Pin-GND	-	±8	-	kV
		OTHER Pin-GND	-	±5	-	kV
	Machine Mode (MM) [2]	OUTn Pin-GND	-	±0.4	-	kV
		OTHER Pin-GND	-	±0.4	-	kV

- [1]The minimum HBM model ESD voltage for all pins complies with the Class-3B standard of JEDEC JS-001-2017 document.
- [2] The minimum MM model ESD voltage for all pins complies with the Class-C standard in JEDEC EIA/JESD22-A115C document.

6.3 Electrical Characteristics

(Unless otherwise specified, VDD=3.5V ~ 5V, Ta=25℃)

Project	Symbol	Test Circuit	Test Condition		Mini Value	Typical Value	Max Value	Unit
REXT voltage characteristics	VR_TT	1	V_{DD}=5V,R_{EXT}=1K IGAIN=100%,T_a=25℃		-	1.510	-	V
	VR_LT		V_{DD}=5V R_{EXT}=1K IGAIN=100%	T_a=-40℃	-	1.503	-	V
	VR_HT			T_a=85℃	-	1.517	-	V
	VR_LV		T_a=25℃ R_{EXT}=1K IGAIN=100%	V_{DD}=5.5V	-	1.51	-	V
	VR_HV			V_{DD}=3.5V	-	1.509	-	V
Constant current output inflection point	V_{OUT1}	2	V_{DD}=5.0V R_{EXT}=1k Inflection point level 0	IOUT=18mA	-	270	-	mV
	V_{OUT2}			IOUT=9mA	-	230	-	mV
	V_{OUT3}			IOUT=4.5mA	-	200	-	mV
	V_{OUT4}		V_{DD}=5.0V R_{EXT}=1k Inflection point level 1	IOUT=18mA	-	300	-	mV
	V_{OUT5}			IOUT=9mA	-	250	-	mV
	V_{OUT6}			IOUT=4.5mA	-	230	-	mV
	V_{OUT7}		V_{DD}=5.0V R_{EXT}=1k Inflection point level 2	IOUT=18mA	-	330	-	mV
	V_{OUT8}			IOUT=9mA	-	280	-	mV
	V_{OUT9}			IOUT=4.5mA	-	250	-	mV
	V_{OUT10}		V_{DD}=5.0V R_{EXT}=1k Inflection point level 3	IOUT=18mA	-	342	-	mV
	V_{OUT11}			IOUT=9mA	-	302	-	mV
	V_{OUT12}			IOUT=4.5mA	-	280	-	mV
	V_{OUT13}		V_{DD}=5.0V R_{EXT}=1k Inflection point level 4	IOUT=18mA	-	420	-	mV
	V_{OUT14}			IOUT=9mA	-	382	-	mV
	V_{OUT15}			IOUT=4.5mA	-	360	-	mV
Constant current source output range	IOUT	2	Inflection point level 0		0.5	-	18	mA
	IOUT1		Inflection point level 1		0.5	-	21	mA
	IOUT2		Inflection point level 2		0.5	-	25	mA
	IOUT3		Inflection point level 3		0.5	-	25	mA
	IOUT4		Inflection point level 4		0.5	-	25	mA
Inter-chip output current error	DCHIP	2	VDS=0.6V		—	±0.2	± 2.0	%
Output current error between channels	DCHL	2	VDS=0.6V		—	± 1.2	±2.0	%
Constant current	%/Δ	2	VDS=0.3~3.0V		—	—	± 1.0	%/V

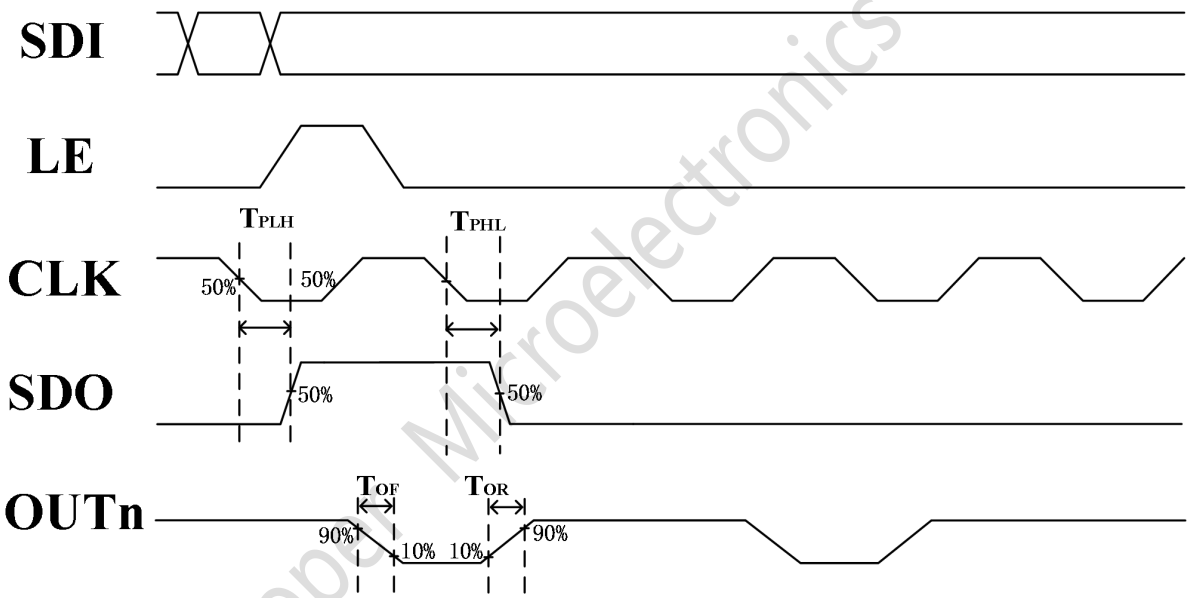
error/VDS variation		VDS						
Constant current error /VDD variation		%/ΔVDD	2	VDD=3.5V~5.0V	—	—	± 1.0	%/V
output voltage at ON		$V_{O(ON)}$	2	OUT0~OUT15	0.3	-	V_{DD}	V
SDO drive current	High Level	IOH	3	VDD=5V	—	-22	—	mA
	Low Level	IOL			—	23	—	mA
Output Level	High Level	VOH	4	IOH=-1mA	4.6	—	—	V
	Low Level	VOL		IOL=1mA	—	—	0.4	V
High level logistic input voltage		V_{IH}	5	-	0.7*V_{DD}	-	V_{DD}	V
Low level logistic input voltage		V_{IL}		-	GND	-	0.3*V_{DD}	V
Supply current (with resistance) (White screen power consumption)		I_{DD1}	6	R_{EXT}=3K，White Screen IOUT=6mA，Refresh rate 3840	-	5.93	-	mA
Supply current (with resistance) (Black screen energy-saving power consumption)		I_{DD3}		R_{EXT}=3K，Black Screen IOUT=6mA,Capability Priority	-	2.72	-	mA
		I_{DD4}		R_{EXT}=3K，Black Screen IOUT=6mA，Low power consumption priority	-	1.84	-	mA
		I_{DD5}		R_{EXT}=3K，Black Screen IOUT=6mA，lowest power consumption	-	0.55	-	mA
Power supply current (no resistance) (White screen power consumption)		I_{DD6}	6	R_{EXT}=3K，White Screen IOUT=6mA，Refresh Rate 3840	-	5.9	-	mA
Power supply current (no resistance) (Black screen energy-saving power consumption)		I_{DD7}		R_{EXT}=3K，Black Screen IOUT=6mA，Capability Priority	-	2.72	-	mA
		I_{DD8}		R_{EXT}=3K，Black Screen IOUT=6mA，Low power consumption priority	-	1.82	-	mA
		I_{DD9}		R_{EXT}=3K，Black Screen IOUT=6mA，lowest power consumption	-	0.55	-	mA

6.4 Dynamic Characteristics

(Unless otherwise specified, VDD=3.5V ~ 5V, Ta=25℃)

Project	Symbol	Test Circuit	Test Condition	Mini Value	Typical Value	Max Value	Unit
CLK-SDO delay	TPHL	7	VDD=5V, FDCLK=12.5MHz	-	50	-	ns
CLK-SDO delay	TPLH			-	50	-	ns
Constant Current Output Rise Time	tOR		I_{OUT}=10mA, ΔV_{OUT}=3V	-	45	-	ns
Constant current output drop time	tOF			-	35	-	ns

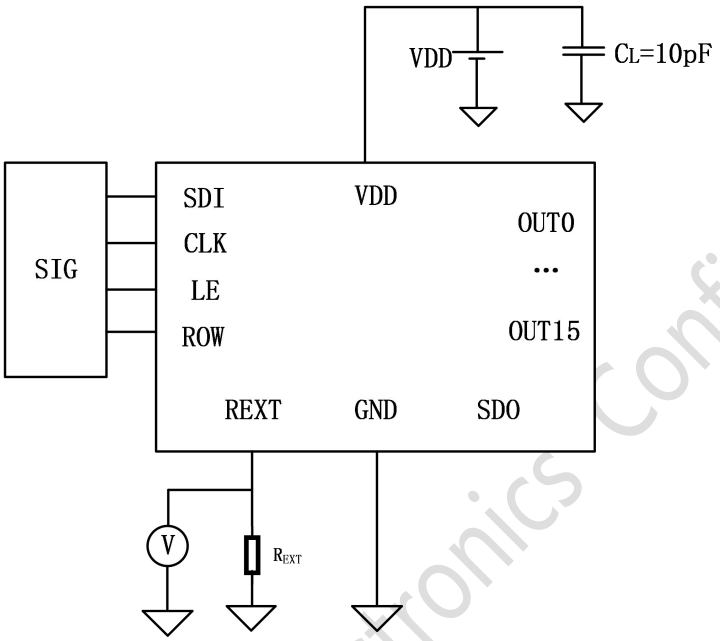
7 Time series waveform diagram



8 Test Circuit Diagram

8.1 Test Circuit 1

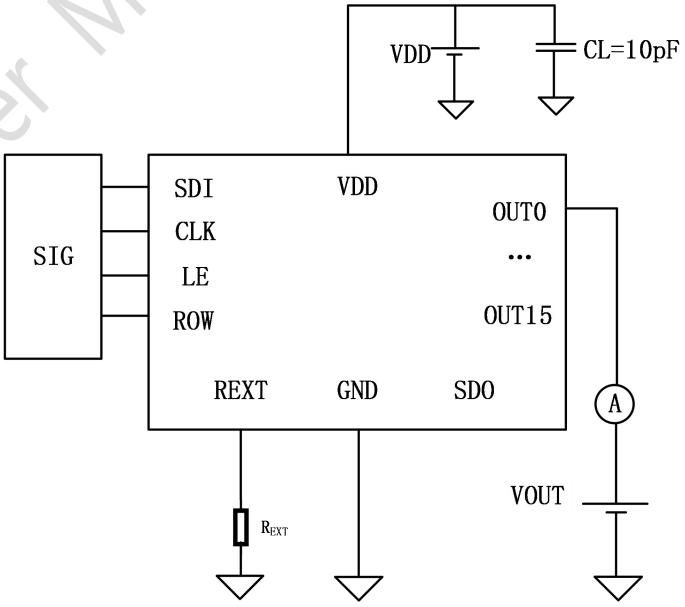
- External resistance voltage



Test circuit 1 schematic diagram

8.2 Test Circuit 2

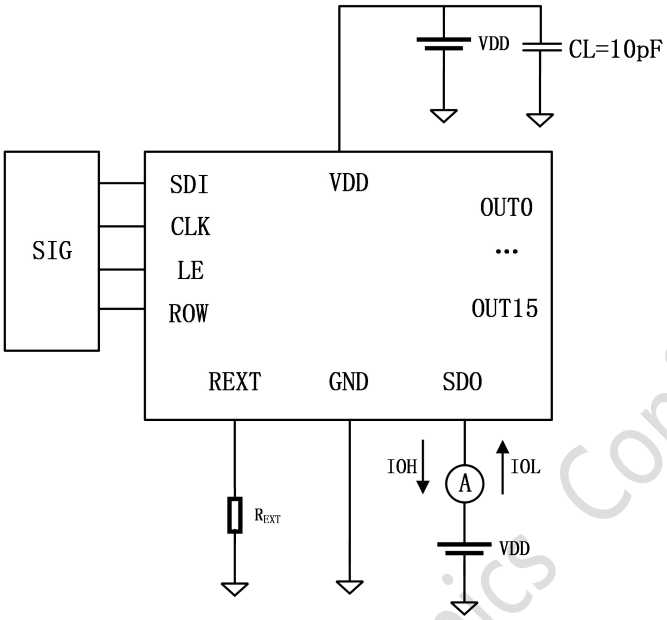
- Constant current output inflection point voltage & corresponding inflection point current (under open circuit detection)



Test circuit 2 schematic diagram

8.3 Test Circuit 3

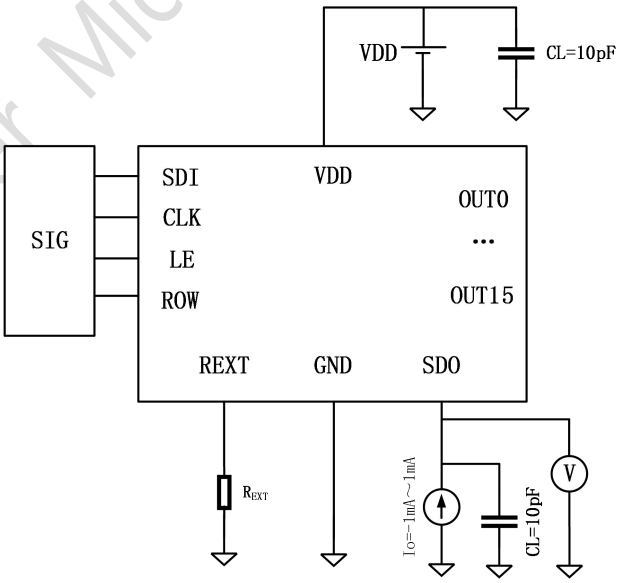
- IOH、IOL



Test circuit 3 schematic diagram

8.4 Test Circuit 4

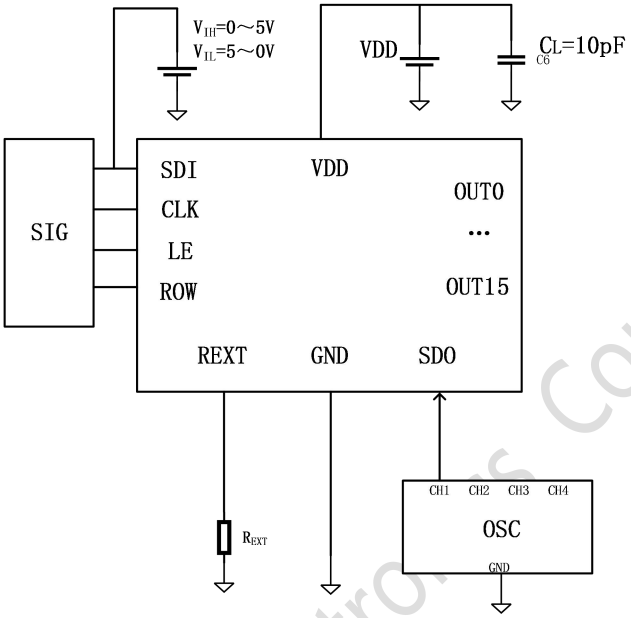
- VOH、VOL



Test circuit 4 schematic diagram

8.5 Test Circuit 5

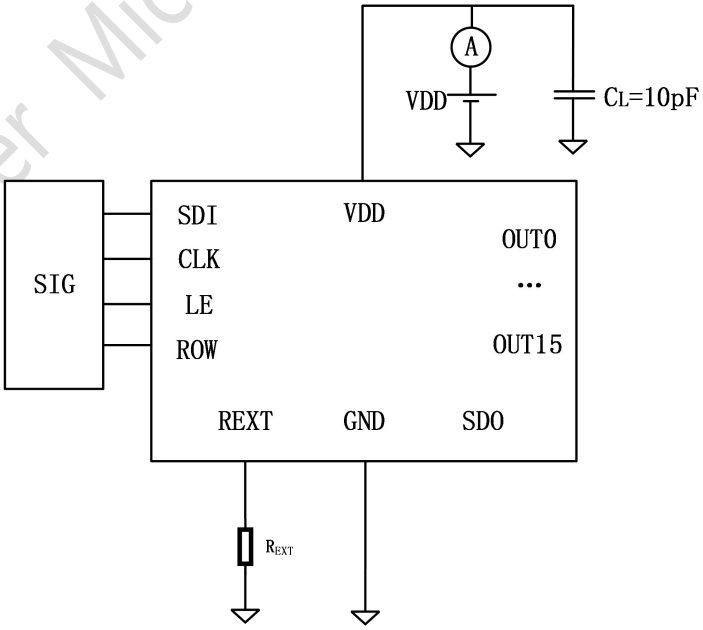
- VIH、VIL



Test circuit 5 schematic diagram

8.6 Test Circuit 6

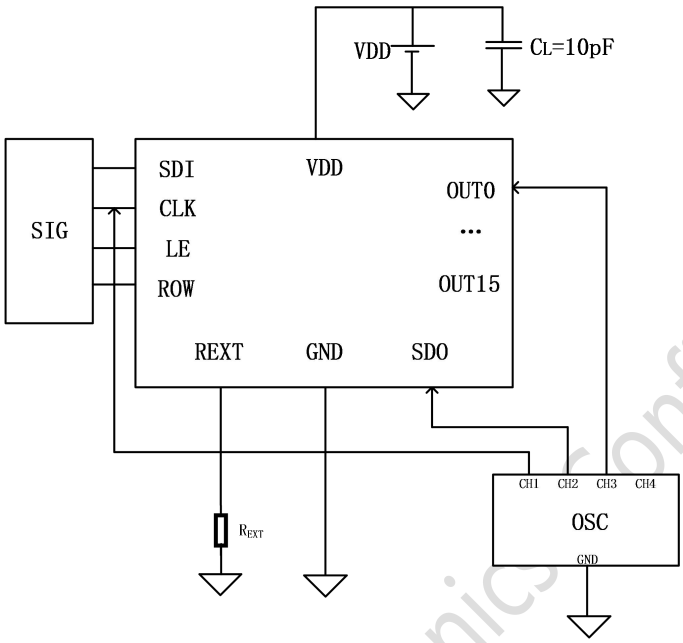
- Power supply current



Test circuit 6 schematic diagram

8.7 Test Circuit 7

- Dynamic Characteristic

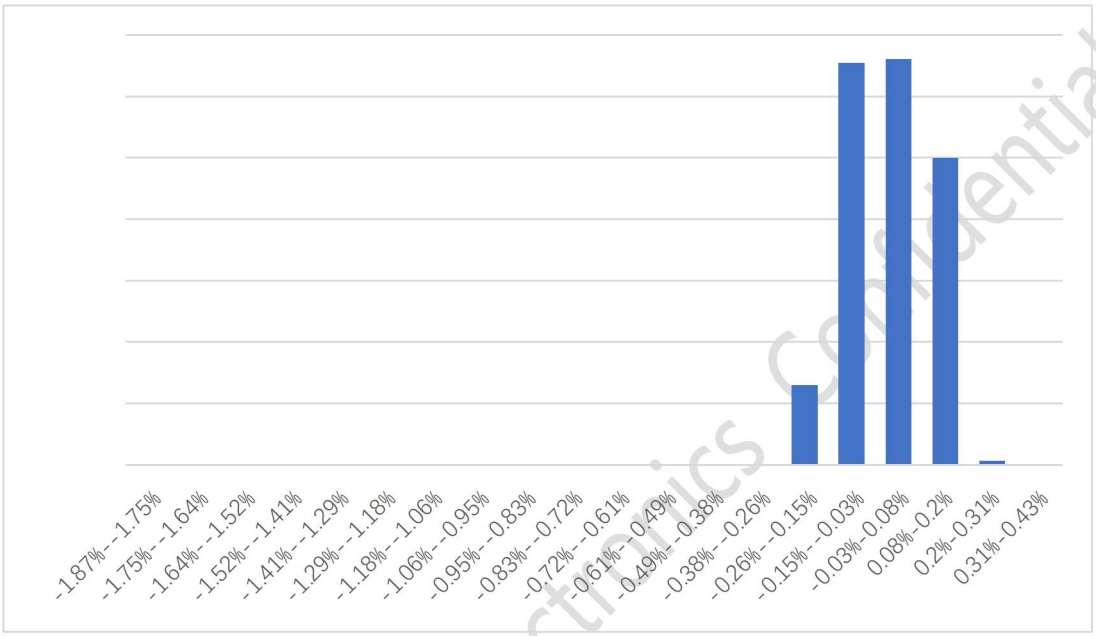


Test circuit 7 schematic diagram

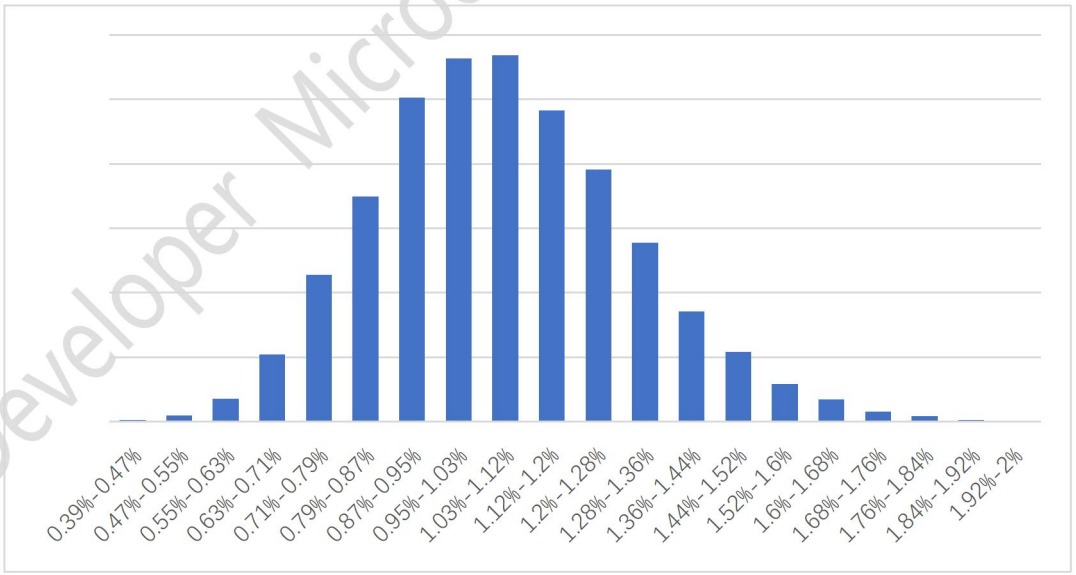
9 Typical Characteristic Diagram

9.1 Constant Current Source Accuracy Test Chart

9.1.1 Inter-chip Current Error



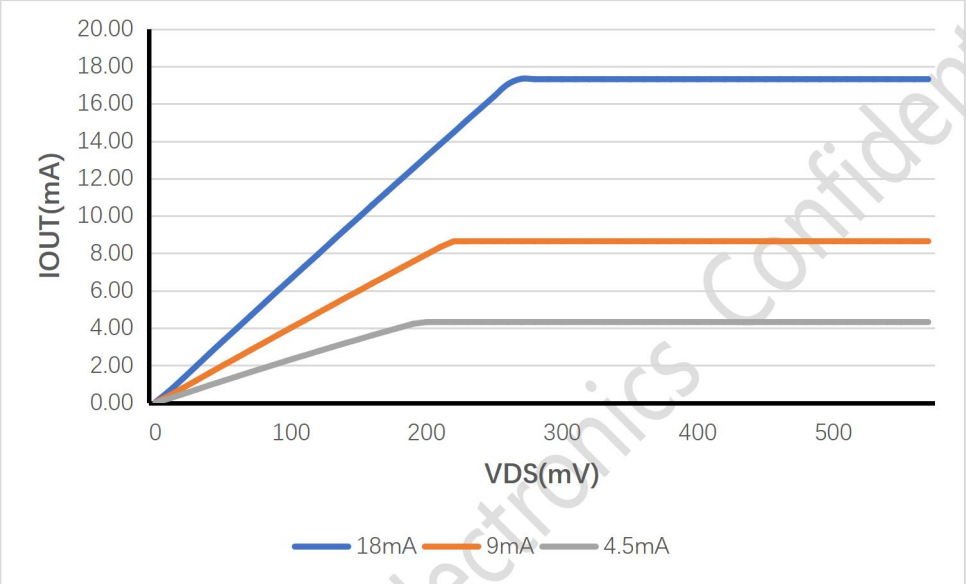
9.1.2 Inter- channel Current Error



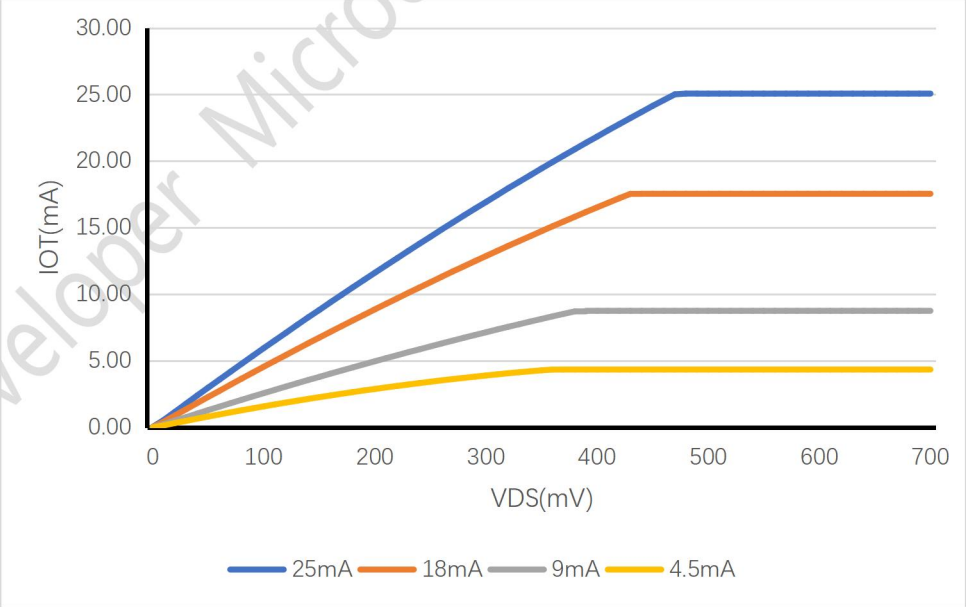
9.2 Constant Current Source Inflection point

When the DP3365S is applied to LED displays, Chip-Chip Skew and channel skew is minimal ,it is due to the DP3365S having excellent constant current output characteristics:

- The maximum channel current error on-chip is less than ±2.0%, and the maximum inter- chip current error is less than ±2.0%;
- When the load terminal voltage (V-out) changes, it is no effect on current output, as shown in the figure below:



In Low inflection Point mode and V_{DD}=5V, I_{OUT} and V_{OUT} relationship curve



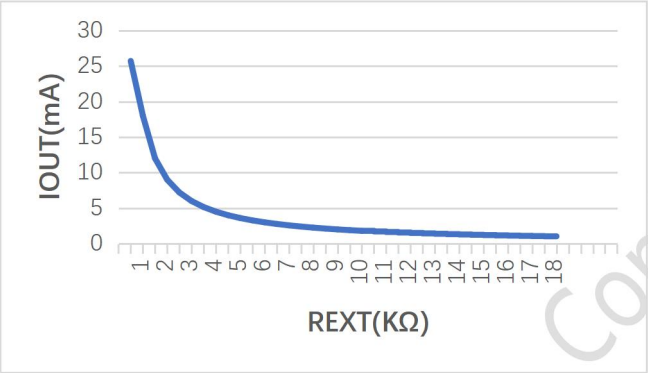
Non- Low inflection Point mode and V_{DD}=5V, I_{OUT} and V_{OUT} relationship curve

9.3 Adjust Output Current by An External Resistance

Output current value is calculated by the following formula:

$$\mathbf{IOUT} = \frac{IGAIN*18}{Rext}\mathbf{,\ 12.5\% \le IGAIN \le 200\%}$$

The REXT in the formula is the resistance value between ground and the chip's 23PIN port. For example, when the current gain IGAIN=100%, REXT=1kΩ, the formula works out the I_{OUT} value 18mA。



IGAIN=100%, REXT and I_{out} relationship curve

10 Typical Display Effect Image

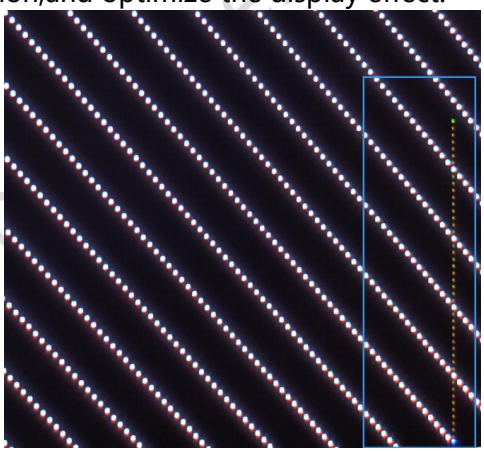
- The specific display effect will be affected by the conditions of the lamp board and register parameters. The following test results are for reference only.

10.1 Display Effect

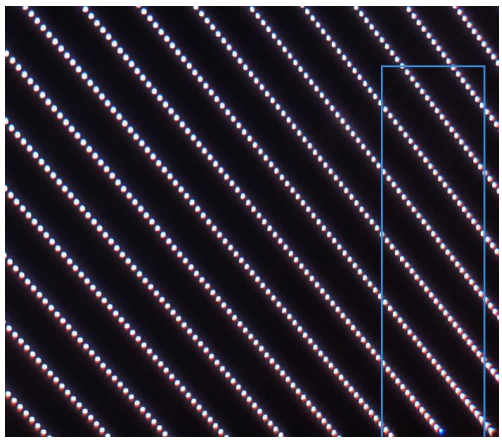
10.1.1 Remove Open Circuit Bad Spot Crosses

The following is a comparison of the display effect before and after removing the open circuit bad spot cross, you can see:

- Chip can remove the bad cross well after opening the function removing the open bad cross function,and optimize the display effect.



Display Effect before Removing open circuit bad spots cross

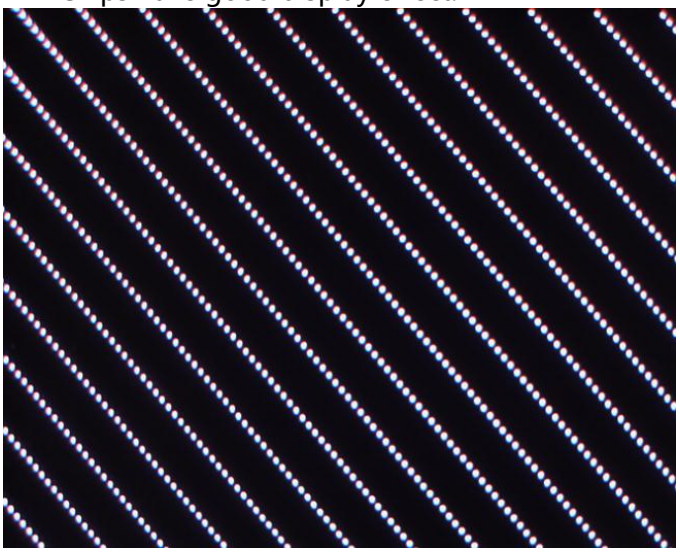


Display effect after removing the open circuit bad spot cross

10.1.2 Remove Ghosting and coupling Effects

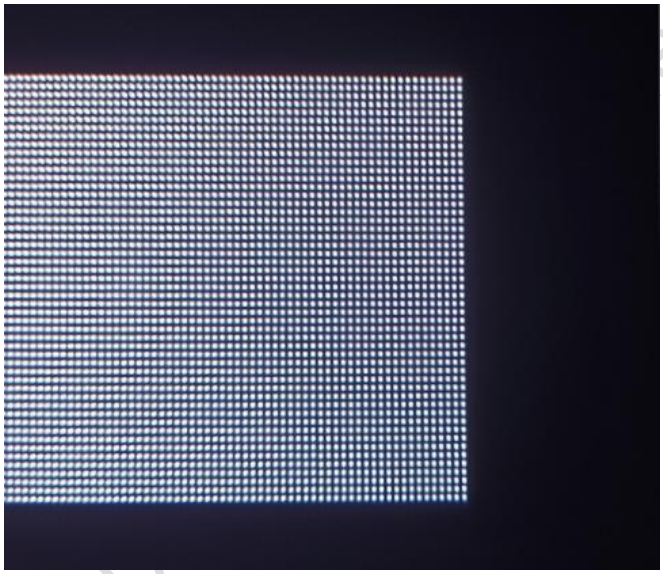
Below is the removal of ghosting and no band lighting effect, you can see:

- Oblique scanning ghost, text ghost and other problems cannot be observed.
- Highlight block with bright, oblique scan superimposed highlight block with bright test results are very good.
- Chips have good display effect.

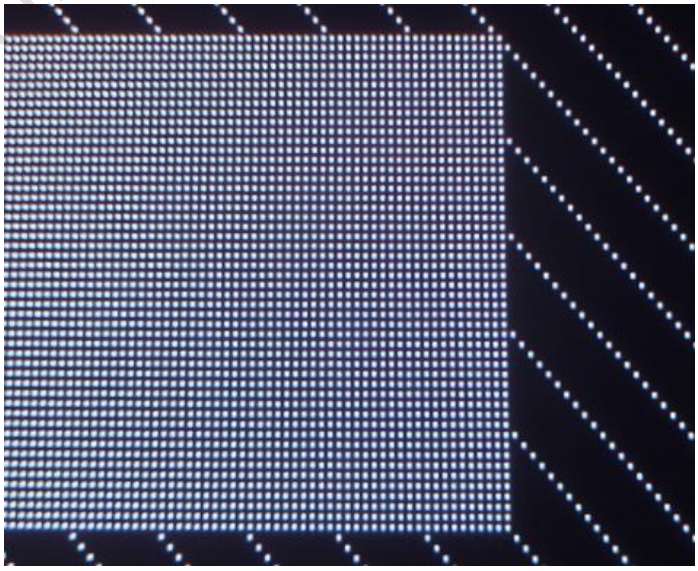


Slanted scan ghosting display effect

Text ghosting test display effect



Highlight block test display effect



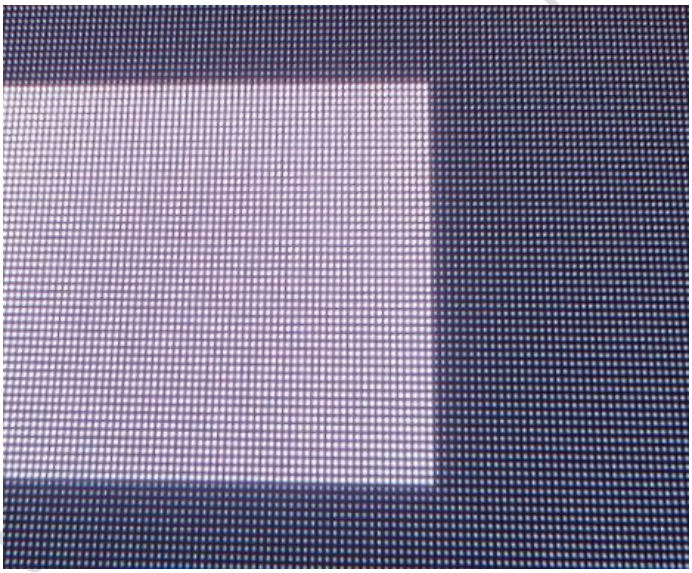
Oblique scan superimposed highlight block with light test display effect

10.1.3 High and low gray interference and coupling display bad effect optimization

The following figure is the optimization effect of high-low gray interference and coupling display poor effects, you can see:

- The low gray coupling of the black block and the low gray coupling of the white block are not sensed.
- Chip shows good display effect.

Black block on the low gray ,coupling test effect



White block on the low gray, coupling test effect

11 Instruction and Register

11.1 Register Instruction

Instruction Name	LE	Description
DATA_LATCH	1	Latch 16bit data to SRAM
VSYNC	3	Update Display Data
WR_CFG	5	Write Register
PRE_ACT	14	Write Enable
DDR	2	Enter Double-edge Mode
SDR	≥15	Enter Single-edge Mode

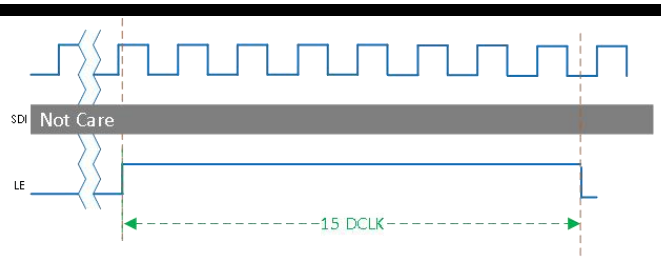
11.2 Data Instructions

Data sending Sequence	Line	Channel
1	Line 0	Channel 15 (OUT15)
2		Channel 14 (OUT14)
.....		.....
16		Channel 0 (OUT0)
17	Line 1	Channel 15 (OUT15)
18		Channel 14 (OUT14)
.....		.....
32		Channel 0 (OUT0)
.....		
1009	Line 63	Channel 15 (OUT15)
1010		Channel 14 (OUT14)
.....		.....
1024		Channel 0 (OUT0)

11.3 Single/Double edge Mode Switch

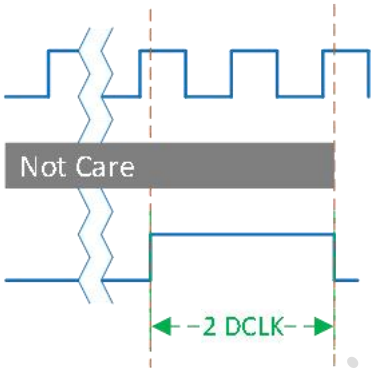
1.Data are collected at the rising edge of the CLK signal in single edge mode; Data are collected at the rising&falling edge of the CLK signal under Double edge mode.

2. The width of OE signal is counted by DCLK signal rising edge;
3.The single/double edge mode switch command needs to be sent one time power-on;
4.Need to enter the single edge mode after power-on, send the command shown in the following figure.



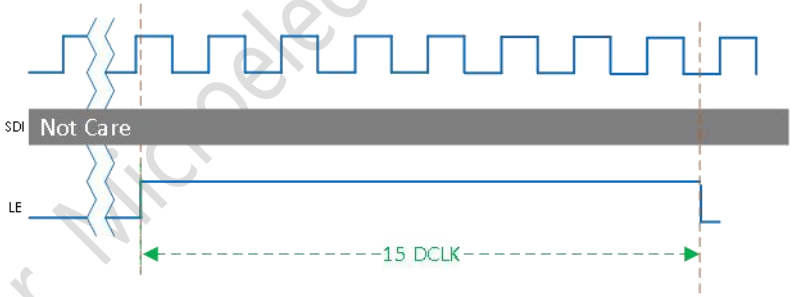
More than or equal to 15 DCLK edges (up + down) are set to SDR

To enter the double-edge mode after power-on, send the command shown in the following figure



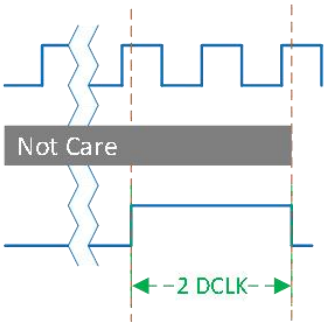
The two DCLK rising edges are set to DDR

★If already in double edge mode and want to enter single edge mode, need to send the following command.



double edge mode, 15 DCLK edges (up + down) are set to SDR

★If already in single edge mode, want to enter double edge mode,need to send the following command.



Single edge mode, the two DCLK rising edges are set to DDR

11.4 Write Register

Send PRE_ACT first, then run WR_CFG, LE is 5 DCLK width, the first input 8bit is the register address bit, the last input 8bit is the data bit of the corresponding register address.

For example:

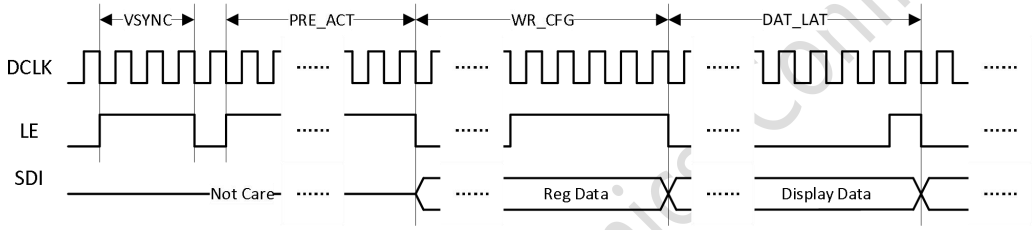
{A7, A6, A5, A4, A3, A2, A1, A0} = 8' b0000_0111;

{D7, D6, D5, D4, D3, D2, D1, D0}=8' b1001_1101;

That is, register 0x07 (8 'b0000_0111) is set to 8' b1001_1101.

11.5 Register Signal Sending Way

The specific driving methods are as follows:



As shown in the figure above, the order of sending instructions and data in each frame:

1. Send VSYNC.
2. Send PRE_ACT.
3. Send WR_CFG and write the register configuration. Each frame can only write a register value of one address for save configuration time.
4. 4.Send multiple LAT signals to cooperate with writing display data.

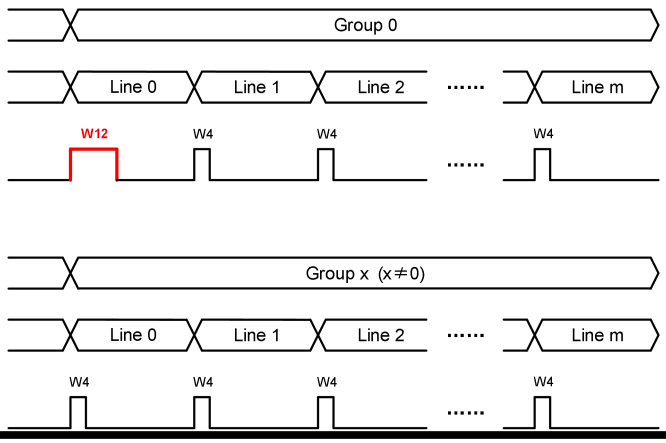
11.6 ROW Signal Sending Way

The DP3365S integrated on-chip GCLK generation circuit changes the OE signal of the universal constant current chip to the ROW signal, using the ROW.

The rising edge of the ROW represents the beginning of a row display, where the high level width of the ROW has two types, namely:

1.W12: The high-level width of the ROW is 12 DCLK width

2.W4: The high-level width of the ROW is 4 DCLK width

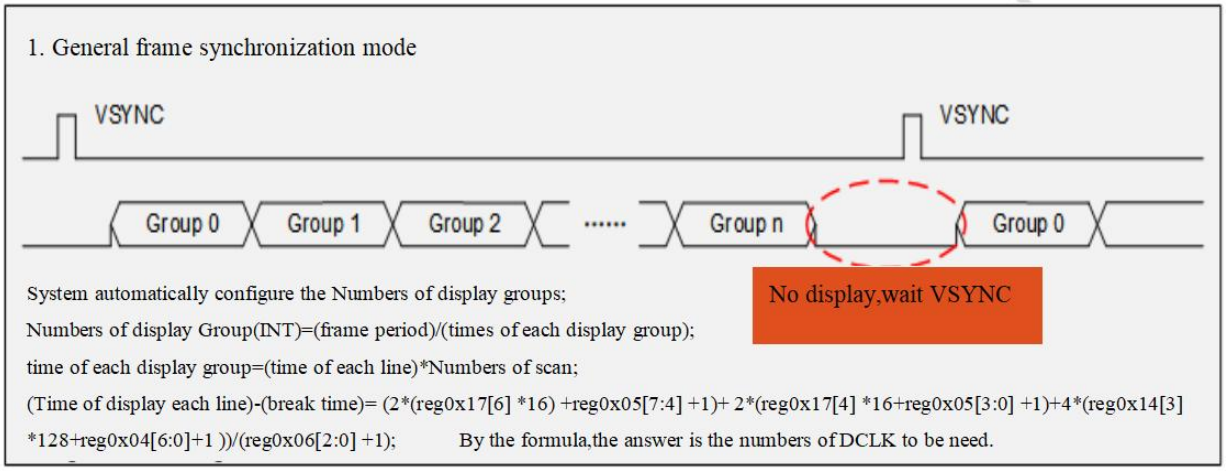


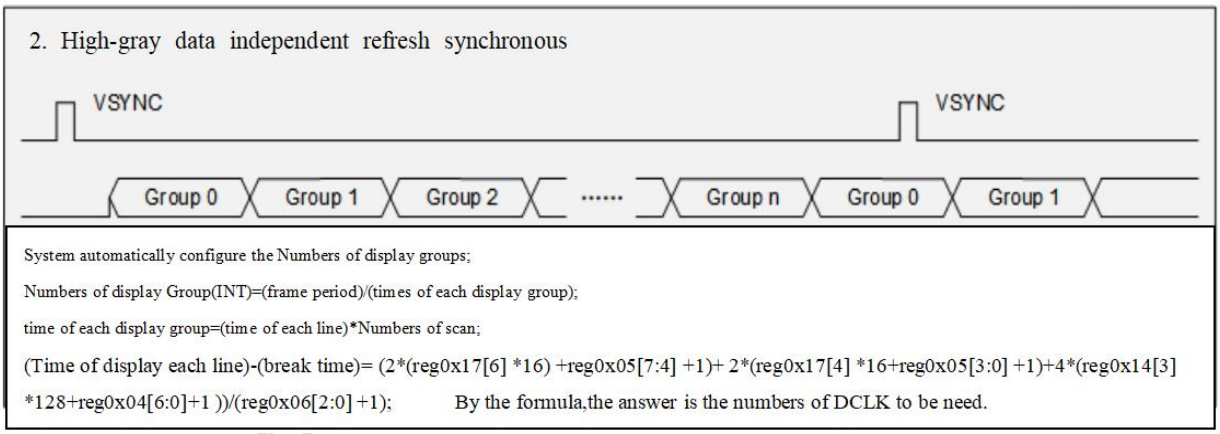
As shown in the figure above, when ROW signals are sent, only the first ROW of Group 1 (Line 0) needs to send ROW signals W12 width, others ROW signals sent W4 width.

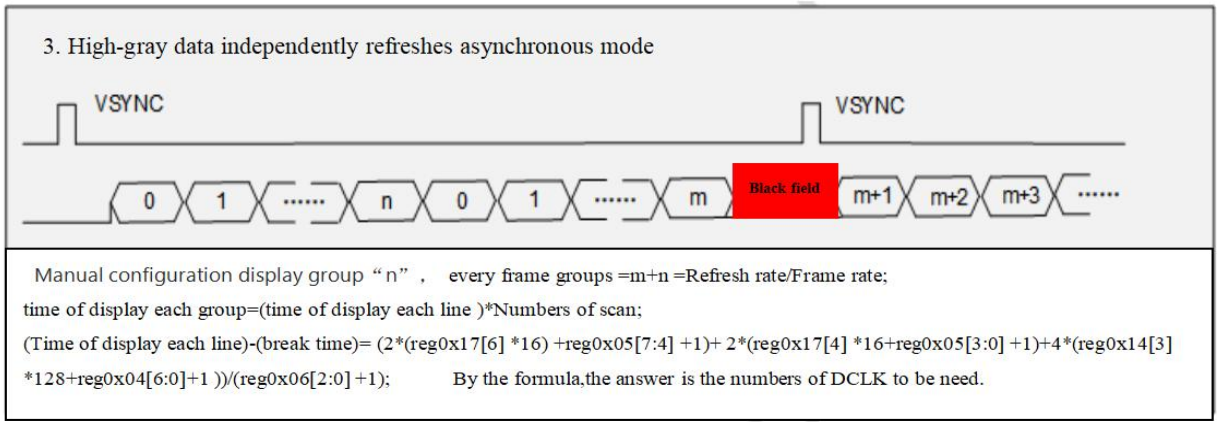
11.7 PWM Display Mode

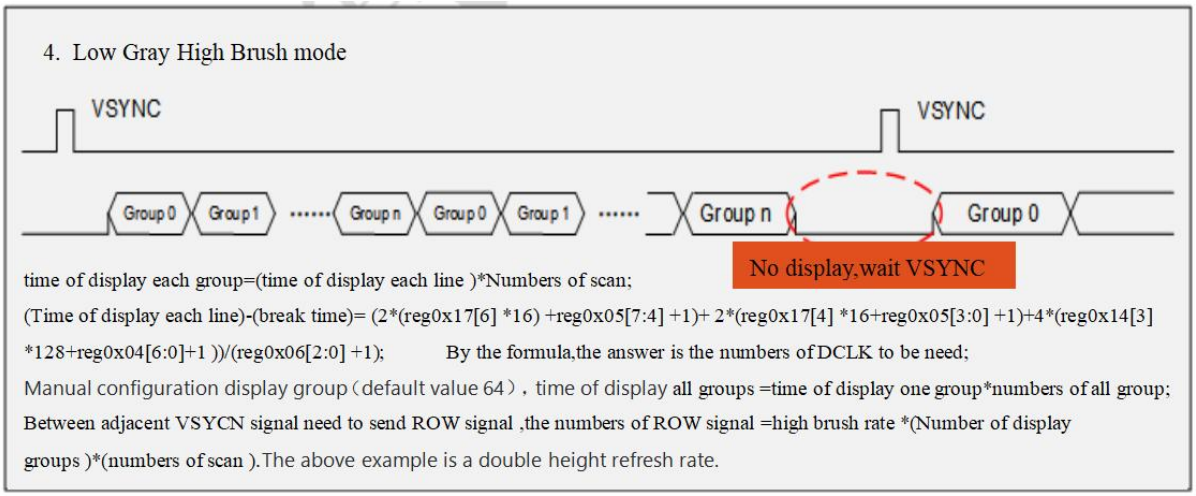
DP3365S integrated four PWM display modes:

1. General frame synchronization mode; 2. High-gray data independent refresh synchronous mode;
3. High-gray data independently refreshes asynchronous mode; 4. Low Ash High Brush mode .









11.7.1 General Frame Synchronization Mode

Working mode and related configurations as follow:

1. Configure reg0X0C [7:6] = 0 and set the PWM display mode to Universal Frame Sync Mode
2. The number of DCLK per line is calculated by the Formula ;
3. The configuration shows the number of data sets, reg0X03[6:0] = refresh rate/frame rate -1
4. After VSYNC,display the first Line (Line 0) of Group 1(Group 0);
5. Stop display the current frame data until the next VSYNC signal coming.

11.7.2 High-gray data independent refresh synchronous mode

Working mode and related configuration:

1. Set the PWM display mode to the high gray data independent refresh frame synchronization mode
2. Calculate a set of display time = frame cycle/(refresh rate/frame rate)
3. Calculate the display time of a row = a group of display time/the number of rows
4. The number of DCLK in each row is calculated according to the formula, which is met by adjusting the gray level of the row, DCLK frequency and register reg0x06[1:0];
5.ROW is continuously transmitted at a fixed display frequency without interruption. The frequency of the ROW is independent of VSYNC. The frequency of the ROW signal = 1/ time of display one line =1/ time of between the rising edges of row signal;
6. ROW 0 of group 0 sends ROW signals of W12. In other cases, ROW signals of W4 are sent. There is only one W12 in every Numbers of row signal , (Numbers of row signal =numbers of groups *numbers of scans) , and it goes on and on and on like this.

11.7.3 High-gray data Independently Refreshes Asynchronous Mode

Working mode and related configuration:

1. Set the PWM display mode to the asynchronous mode of high gray data independent refresh
2. The number of DCLKS in each row is calculated according to the formula

3. Display the number of data groups manually. The default value is 64 groups (reg0x03[6:0]=7 'h3f), and a maximum of 128 groups are supported.
4.ROW signal frequency = 1/time of display one line = 1/time between rising edges of row signal
5. The numbers of group to be displayed in a frame = display refresh rate/frame rate, and the numbers of groups to be displayed in a frame can be greater than the number of data groups configured in Step 3. In this case, the control card needs to send (display refresh rate/frame rate * number of lines) ROW signals in a frame, and the state of inter frame black field is displayed until the next VSYNC coming.
6. ROW 0 of group 0 sends ROW signals of W12. In other cases, ROW signals of W4 are sent. There is only one W12 in every Numbers of row signal , (Numbers of row signal =numbers of groups *numbers of scans) , and it goes on and on and on like this.
7. In asynchronous mode, the refresh rate can be greater than 7680.

Descriptions:

The main differences between synchronous mode and asynchronous mode are:
1. Independent refresh frame synchronization mode for high gray data: The number of display data groups is automatically configured according to the display frame time.
2. Independent refresh of high gray data Asynchronous mode: The numbers of display group can be manually configured.

11.7.4 low gray and high brush mode

Working mode and related configuration:
1. Set PWM display mode to low gray and high brush mode
2. The number of groups displayed is manually configured (the default is 64 groups).
3. The number of DCLK in each row is calculated according to the formula, and the display time of a row is calculated
4. Calculate a group display time = a row display time x the number of rows
5. Calculate all group display time = one group display time * Number of groups,
6. High brush rate (rounded) = frame cycle/display time of all groups
7. Two VSYNC need to send Numbers of row signal =high brush rate * numbers of display group * Numbers of scan;
8. Display the first Line (Line 0) of the first Group 1 (Group 0) after VSYNC
9. when Completed all data groups display , in the high brush setting ,then stop display ; until the next VSYNC coming, continue to display;
10. Visual refresh rate = frame rate * numbers of group * High brush rate;
11. The low gray and high brush mode only needs to change the ROW signal according to the above steps, and the gray level does not need to be adjusted

11.8 Relevant Configuration of PWM Display

11.8.1 Number of Row Scans Configured

DP3365S supports up to 64 line scans, configured as reg0x02[5:0] = number of line scans -1

11.8.2 Row Grayscale Configuration

reg0x14[3]*128+reg0x04[6:0] represents the PWM display length of a row, the PWM display length of a

row = 4*(reg0x14[3]*128+reg0x04[6:0]+1), the maximum support line gray level 256X4=1024;

11.8.3 PWM Display Packet Configuration

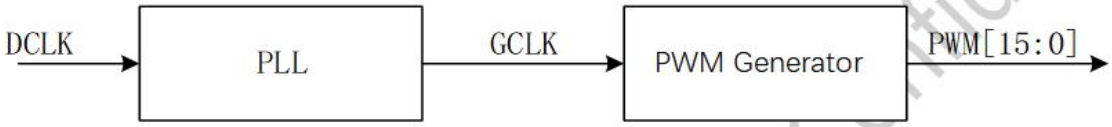
reg0x03[6:0] indicates the number of PWM display packets. The numbers of PWM display group = reg0x03[6:0]+1. The maximum numbers of supported group is 128;

In frame synchronization mode, PWM displays the numbers of group = refresh rate/frame rate

In asynchronous mode, PWM display group can be configured independently (independent of refresh rate)

The number of group is less than or equal to the maximum number of packets. The DP3365S supports two maximum number of packets, 128 and 64.

11.8.4 Internal Grayscale Clock Configuration



DP3365S integrates PLL on chip to produce gray clock GCLK. The relevant calculation formula is as follows:

FGCLK=FDCLK* Frequency division coefficient

11.8.5 PWM Gray scales Series & Gamma Generation

PWM gray level (maximum)= Line gray level *PWM display group

Gamma can be calculated and generated according to the PWM gray level (maximum) (this part is generated by the control card manufacturer according to their own gamma generation formula)

The maximum chip gray level supports 16bit.

11.9 Open Circuit Detection and Removal of Bad Spots

Selected【Remove bad spots】: reg0x0c[1]=1 ;

Non-selected【Remove bad spots】: reg0x0c[1]=0

12 Package cooling power(P_D)

The maximum heat dissipation power of the encapsulation is determined by the formula: $P_{D(\max)} = \frac{(T_j - T_a)}{R_{th(j-a)}}$

When all 16 channels are open, the actual power is:

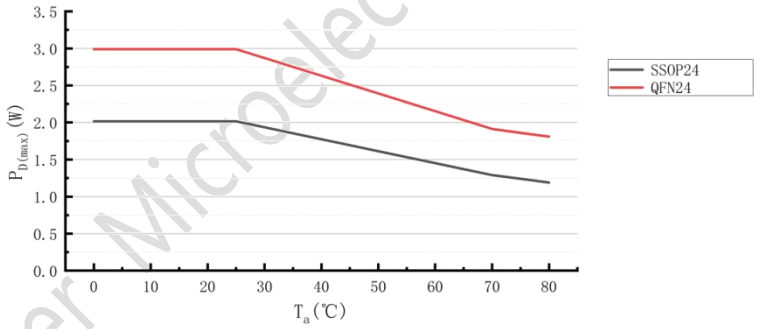
$P_{D(act)} = I_{DD} * V_{DD} + I_{OUT} * Duty * V_{DS} * 16$

To ensure that $P_{D(act)} \leq P_{D(max)}$ output maximum current and duty cycle relationship is:

$$I_{OUT(max)} = \frac{\frac{T_j - T_a}{R_{th(j-a)}} - (I_{DD} * V_{DD})}{V_{DS} * Duty * 16}$$

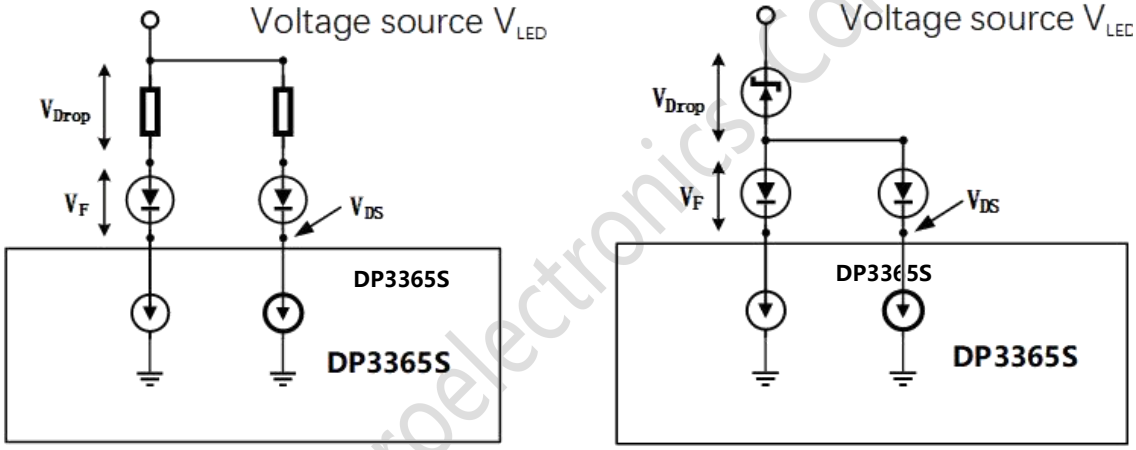
Therein T_j is the junction temperature (T_j=150℃), T_a is the ambient temperature, V_{DS} is the constant current output port voltage, Duty is the duty cycle, and $R_{th(j-a)}$ is the thermal resistance of the encapsulation.

封装	$R_{th(j-a)}$(℃/W)	$P_{D(max)}$(W)
QSOP24	62	2.01
QFN24	41.8	2.99



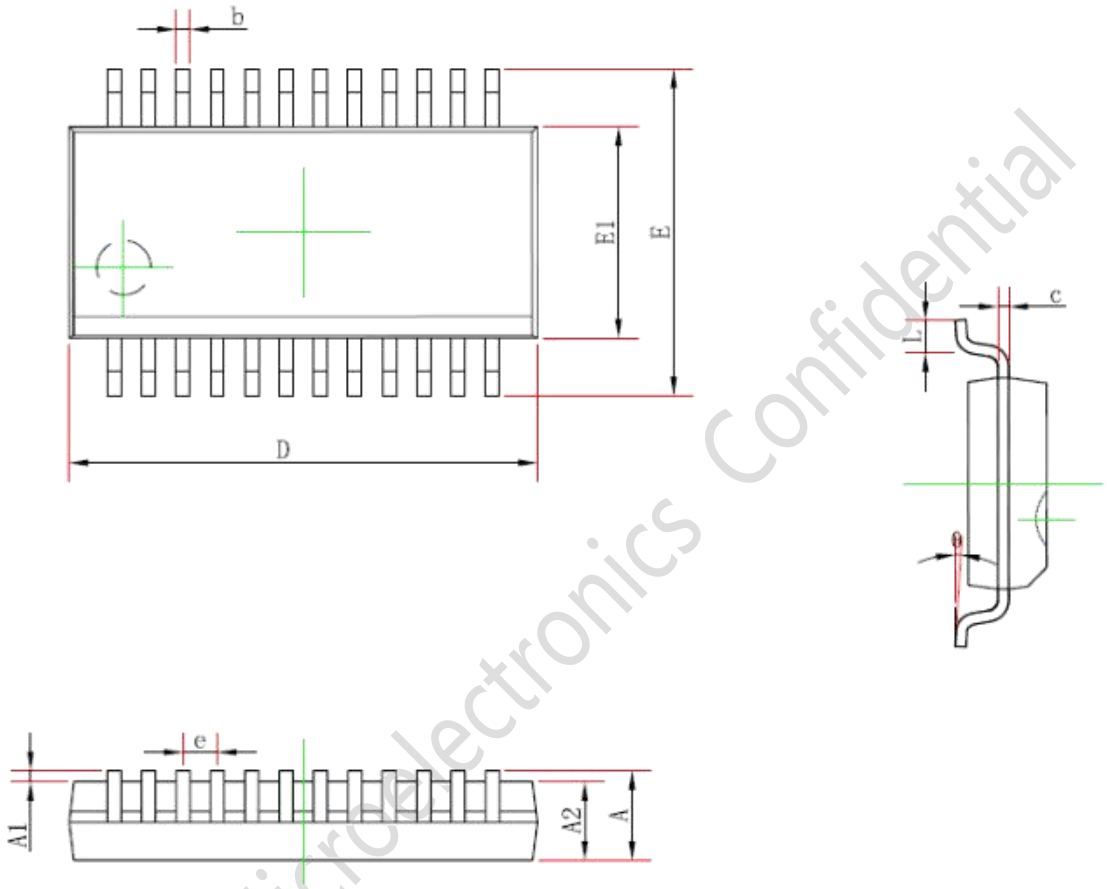
13 Load Terminal Voltage(VLED)

In order to optimize the heat dissipation capacity of the package, it is recommended that the best operating range of the output terminal voltage (V_{DS}) is 0.3V to 1.0V(I_{OUT}= 0.5-36mA). If $V_{DS}=V_{LED}-V_F$ and V_{LED}=5V, the high output voltage (V_{DS}) may cause PD (act) > PD (max); In this case, it is recommended to use the lowest possible V_{LED} voltage for use, and an external resistor or voltage regulator can also be used as a V_{DROP}. This results in $V_{DS}=(V_{LED}-V_F)-V_{DROP}$, which reduces the input voltage (V_{DS}) value. The application diagram of the external series resistor or voltage regulator can be referred to the following figure.



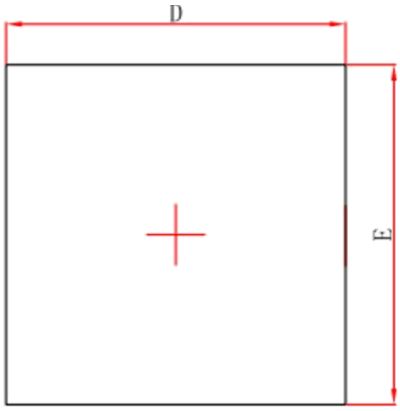
14 Encapsulation Information

- QSOP24 Plastic Encapsulation Specification Drawing

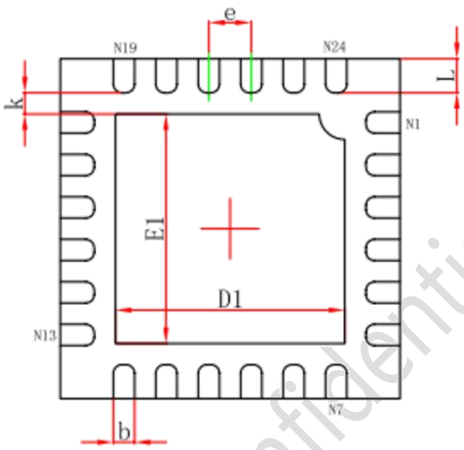


	Millimeters (mm)	
	Min	Max
A	—	1.95
A1	0.05	0.35
A2	1.05	—
b	0.1	0.4
c	0.05	0.254
D	8.2	9.2
E1	3.6	4.2
E	5.6	6.5
e	0.635TYP	
L	0.3	1.5
θ	0°	10°

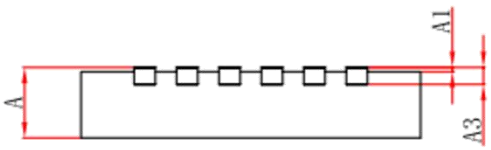
- QFN24 Plastic Encapsulation Specification Drawing



Top View



Bottom View



Side View

	Millimeters (mm)	
	Min	Max
A	0.700/0.800	0.800/0.900
A1	0.000	0.050
A3	0.203REF	
D	3.924	4.076
E	3.924	4.076
D1	2.6	2.8
E1	2.6	2.8
k	0.20MIN	
b	0.200	0.300
e	0.500TYP	
L	0.324	0.476

15 Official Announcement

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