Common Cathode16-Channel PWM Constant Current LED Sink IC

1 Product overview

DP3269 is a PWM constant current sink LED chip for LED display with low turning point, integrated high-precision current generation circuit technology, to achieve chip-to-chip current error less than 2.0%, and with variety exclusive technology to improve the LED display effect, bring more development in LED display field.

2 Characteristic

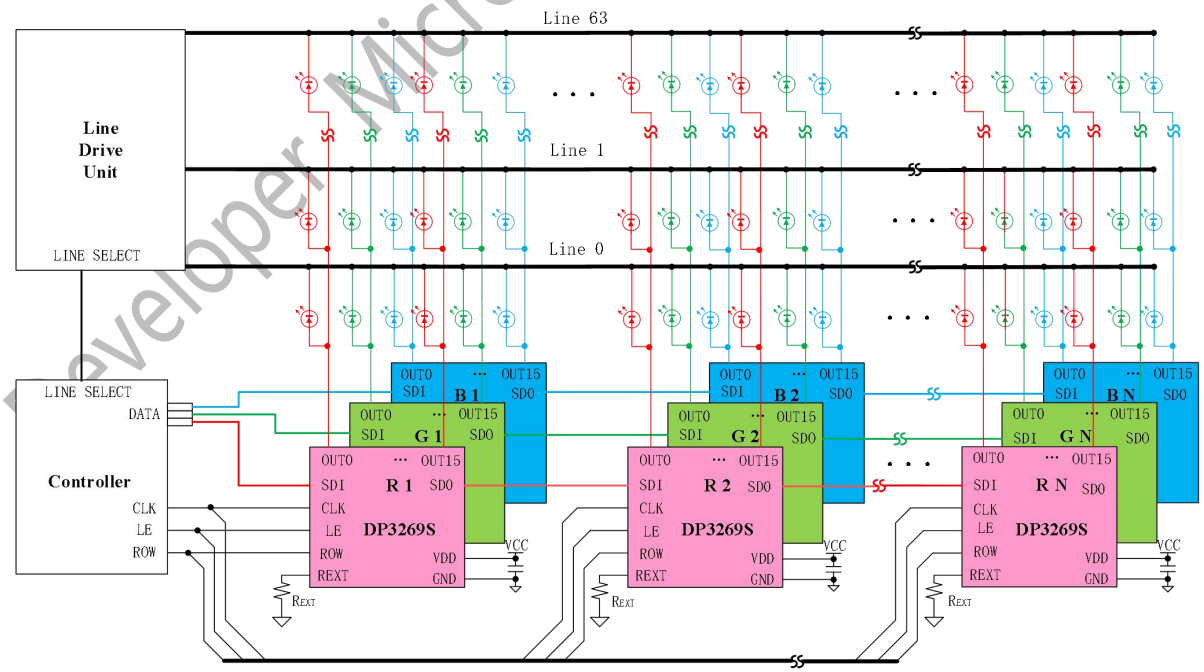
- Voltage range：2.6V～5.5V
- Working temperature：-40℃～85℃
- Scans ：1～64 scans，Adjustable
- 16 channels output constant current
- constant current output range
  - 0.5mA～18mA (V_{out}=0.3V)
  - 0.5mA～36mA (V_{out}=0.6V)
- Current error between channels
  Typical value：±1.0% Maximum value ：±2.0%
- Current error between Chips
  Typical value：±0.2% Maximum value：±2.0%
- High gray independent display / High display refresh rate
- Optimizing display effect
  - Improve low gray uniformity
  - Improve the first line with dim condition
  - Improve ghost
  - Improve coupling when white block and black block overlay the low gray
  - Improve coupling between modules
- Integrated PLL to be GCLK and to be compared with external GCLK, Frequency range is wider,and EMI is lower.

Package type：QSOP24/QFN24

- More higher ESD class

3 Application field

- High refresh rate full-Color display
- Supply high density and small space LED display module



DP3269S Typical application

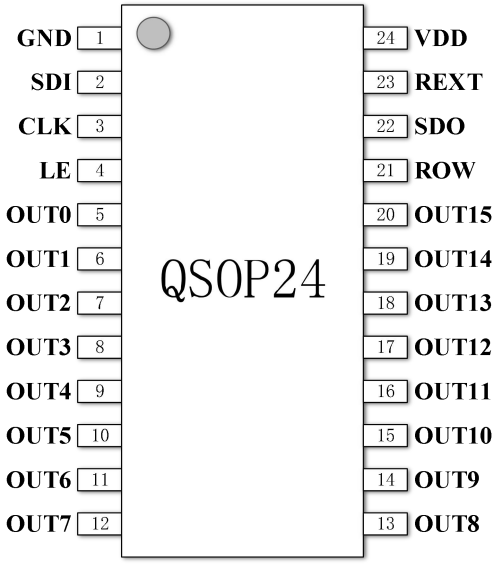
目录

Revise history

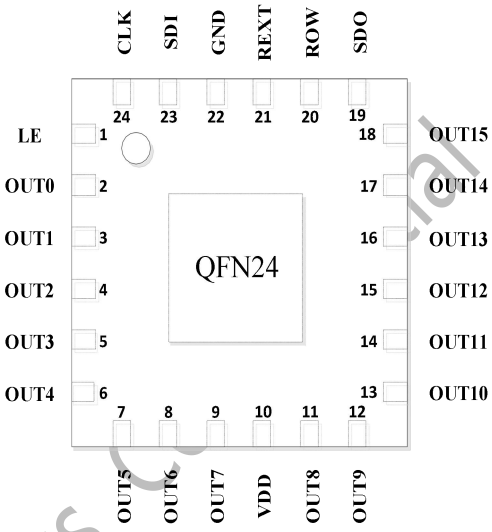
Version NO.	Revision date	Reviser	Revise Content
V1.0	2023.03	Guan YiCheng	**Original Version**
V2.0	2024.02	Wang Mei	Update document structure Add new contents: 1. Revision Description 2. Test circuit diagram 3. Time series waveform diagram 4. Typical characteristic 5. Display effect 6. Instruction and register 7. Encapsulation Cooling Power (PD) 8. Load port Voltage

4 Product Description

- pin definition



QSOP24



QFN24

- Pin Description

QSOP24 PIN Number	QFN24 PIN Number	PIN Name	PIN Description
1	22	GND	Power Ground
2	23	SDI	Serial data input
3	24	CLK	Clock input terminal for data shift and command information
4	1	LE	Data transfer command input
5 ~ 20	2 ~ 9 11 ~ 18	OUT0 ~ OUT15	Constant current output
21	20	ROW	Scan Line change signal
22	19	SDO	Serial data output
23	21	REXT	Constant-current value setting .Connection to an external resistor to GND
24	10	VDD	Power-supply voltage

- ORDERING INFORMATION

Product Name	Package type	Package mode	number/reel	humidity sensitivity class
DP3269S	QSOP24	Tape	4000	MSL=3
	QFN24	Tape	5000	

- Product marking

QSOP24

QFN24

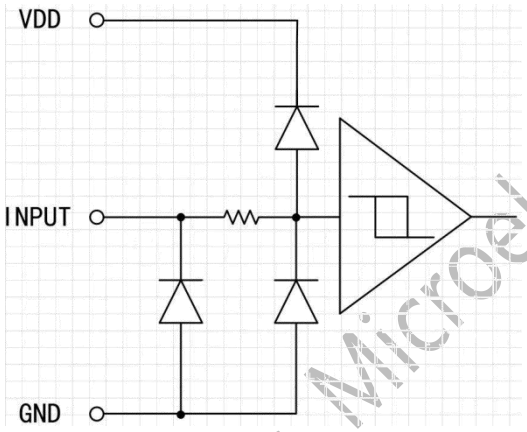
DP3269S is the product name.

XXXXXX Represents the product batch number.

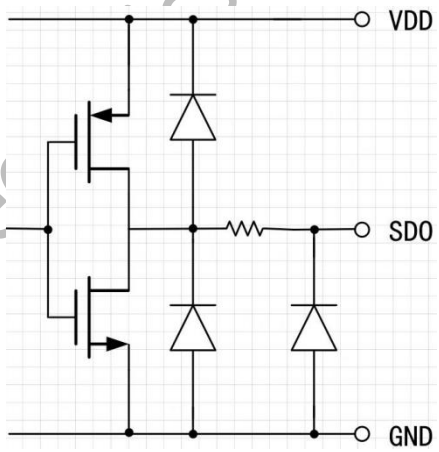
5 Circuit Schematic Diagram

5.1 OUT/PUT equivalent circuit

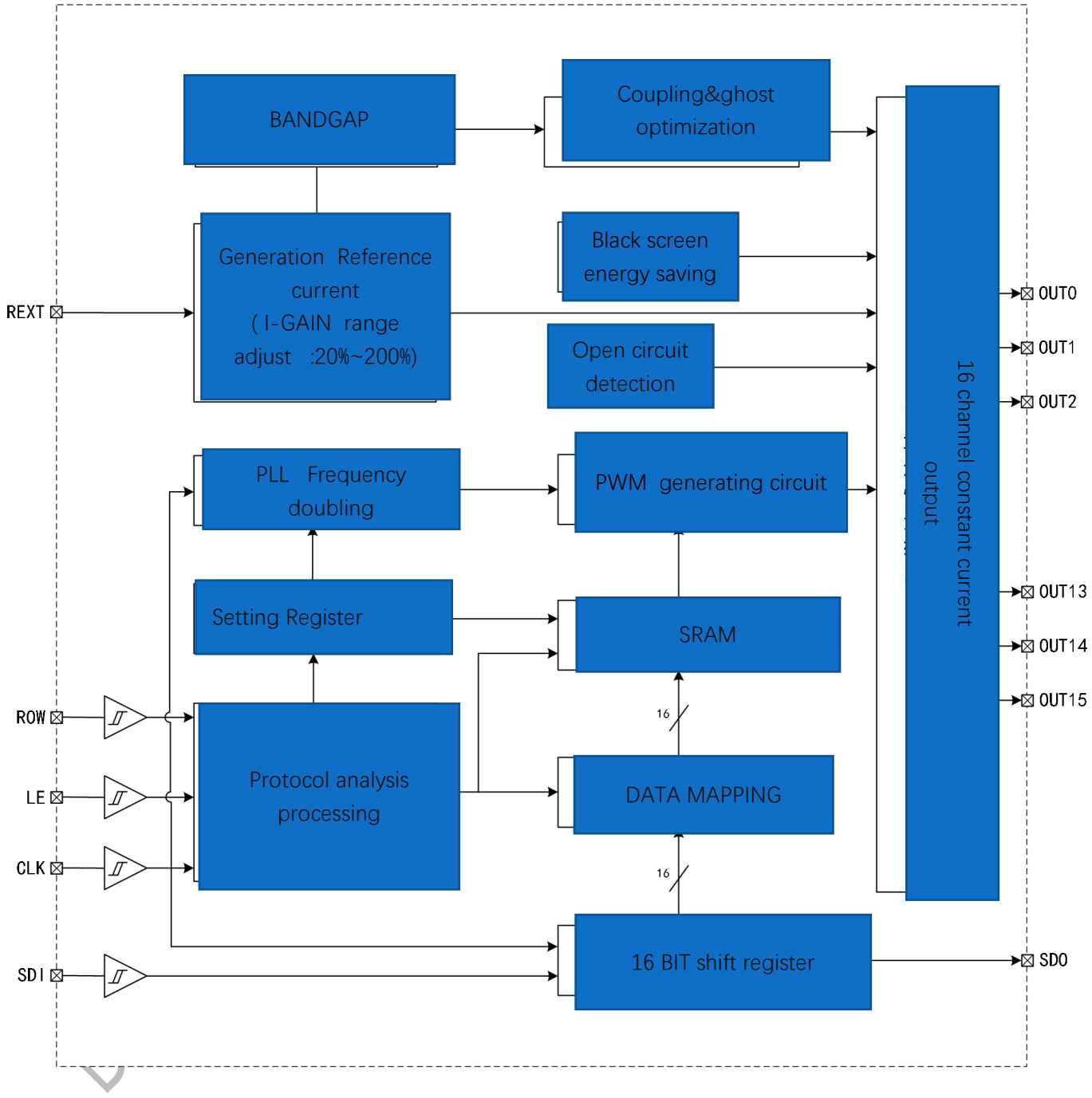
SDI,CLK,LE,OE INPUT



SDO OUTPUT



5.2 Internal Circuit Block Diagram



Internal circuit diagram

6 Parameter List

6.1 Maximum Limit Parameter

Project	Symbol	Rated Value	Unit
Supply Voltage	V_{DD}	0 ~ 6	V
Output Current	I_O	36	mA
Input Voltage	V_{IN}	-0.4 ~ V_{DD}+0.4	V
Output withstand voltage	V_{OUT}	11	V
clock frequency	F_{CLK}	25	MHz
Operating Temperature	T_{opr}	-40 ~ 85	℃
Storage Temperature	T_{stg}	-55 ~ 150	℃

- All voltage values are based on the chip grounding terminal (GND) as a reference point, and the test temperature for the maximum limit parameter is 25℃.
- If the actual working conditions exceed the specified value may cause permanent damage to the components; If the actual operating conditions are slightly below the maximum and work for a long time, the reliability of the component may be reduced. The above values are only partially specified, and this product does not support functional operation under other conditions outside the specifications.
- The maximum peak welding temperature of surface paste products shall not exceed 260℃. The temperature curve shall be set by the factory according to J-STD-020 standard, the actual situation of the factory and the solder paste manufacturer's suggestion.

6.2 Electrical Characteristics (Unless otherwise specified,VDD=3.5V～5V，Ta=25℃)

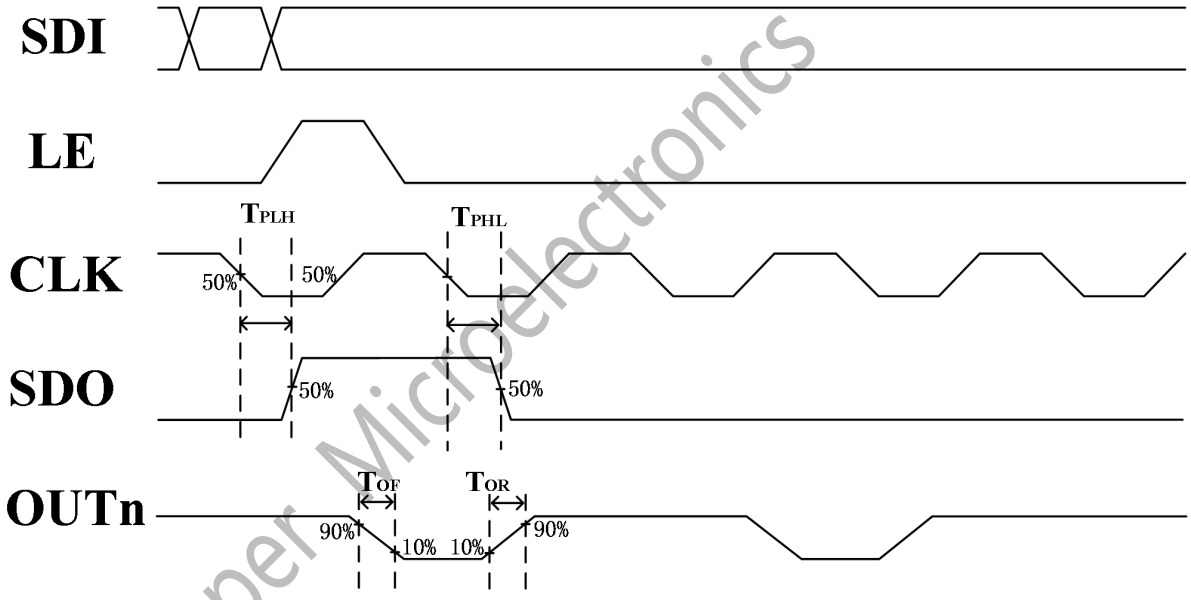
Project	Symbol	Test Circuit	Test Condition		Mini Value	Typical Value	Max Value	Unit
REXT voltage characteristics	VR_TT	1	V_{DD}=5V,R_{EXT}=1K IGAIN=100%,T_a=25℃		0.948	0.985	1.129	V
	VR_LT		V_{DD}=5V R_{EXT}=1K IGAIN=100%	T_a=-40℃	-	0.973	-	V
	VR_HT			T_a=85℃	-	0.994	-	V
	VR_LV		T_a=25℃ R_{EXT}=1K IGAIN=100%	V_{DD}=5.5V	-	0.988	-	V
	VR_HV			V_{DD}=3.5V	-	0.981	-	V
Constant current output inflection point	V_{OUT1}	2	V_{DD}=5.0V R_{EXT}=1k inflection point grade0	IOUT=18mA	-	310	-	mV
	V_{OUT2}			IOUT=9mA	-	240	-	mV
	V_{OUT3}			IOUT=4.5mA	-	210	-	mV
	V_{OUT4}		V_{DD}=5.0V R_{EXT}=1k inflection point grade1	IOUT=18mA	-	330	-	mV
	V_{OUT5}			IOUT=9mA	-	310	-	mV
	V_{OUT6}			IOUT=4.5mA	-	240	-	mV
	V_{OUT7}		V_{DD}=5.0V R_{EXT}=1k inflection point grade2	IOUT=18mA	-	360	-	mV
	V_{OUT8}			IOUT=9mA	-	320	-	mV
	V_{OUT9}			IOUT=4.5mA	-	270	-	mV
	V_{OUT10}		V_{DD}=5.0V R_{EXT}=1k inflection point grade3	IOUT=18mA	-	420	-	mV
	V_{OUT11}			IOUT=9mA	-	350	-	mV
	V_{OUT12}			IOUT=4.5mA	-	300s	-	mV
	V_{OUT13}		V_{DD}=5.0V R_{EXT}=1k inflection point grade4	IOUT=18mA	-	560	-	mV
	V_{OUT14}			IOUT=9mA	-	440	-	mV
	V_{OUT15}			IOUT=4.5mA	-	380	-	mV
Constant current source output range	IOUT	2	inflection point grade0		0.5	-	18	mA
	IOUT1		inflection point grade1		0.5	-	21	mA
	IOUT2		inflection point grade2		0.5	-	25	mA

		IOUT3		inflection point grade3	0.5	-	30	mA
		IOUT4		inflection point grade4	0.5	-	36	mA
Inter-chip output current error		DCHIP	2	VDS=0.6V	—	±0.2	± 2.0	%
Output current error between channels		DCHL	2	VDS=0.6V	—	± 1.0	±2.0	%
Constant current error/VDS variation		%/Δ VDS	2	VDS=0.3~3.0V	—	—	± 1.0	%/V
Constant current error /VDD variation		%/Δ VDD	2	VDD=3.5V~5.0V	—	—	± 1.0	%/V
output voltage at ON		$V_{O(ON)}$	2	OUT0~OUT15	0.3	-	V_{DD}	V
SDO drive current	High Level	IOH	3	VDD=5V	—	-22	—	mA
	Low Level	IOL			—	23	—	mA
Output Level	High Level	VOH	4	IOH=-1mA	4.6	—	—	V
	Low Level	VOL		IOL=1mA	—	—	0.4	V
High level logistic input voltage		V_{IH}	5	-	0.7*V_{DD}	-	V_{DD}	V
Low level logistic input voltage		V_{IL}		-	GND	-	0.3*V_{DD}	V
Supply current (with resistance) (White screen power consumption)		I_{DD1}	6	R_{EXT}=3K, White Screen IOUT=6mA, Refresh rate 3840	-	5.62	-	mA
Supply current (with resistance) (Black screen energy-saving power consumption)		I_{DD3}	6	R_{EXT}=3K, Black Screen IOUT=6mA, Capability Priority	-	3.41	-	mA
		I_{DD4}		R_{EXT}=3K, Black Screen IOUT=6mA, Low power consumption priority	-	1.2	-	mA
		I_{DD5}		R_{EXT}=3K, Black Screen IOUT=6mA, lowest power consumption	-	0.41	-	mA

6.3 Dynamic Characteristics (Unless otherwise specified,VDD=3.5V～5V，Ta=25℃)

Project	Symbol	Test Circuit	Test Condition	Mini Value	Typical Value	Max Value	Unit
CLK-SDO delay	TPHL	7	VDD=5V, FDCLK=12.5MHz	-	50	-	ns
CLK-SDO delay	TPLH		VDD=5V, FDCLK=12.5MHz	-	50	-	ns
Constant Current Output Rise Time	tOR		IOUT=10mA, ΔVOUT=3V	-	45	-	ns
Constant current output drop time	tOF		IOUT=10mA, ΔVOUT=3V	-	35	-	ns

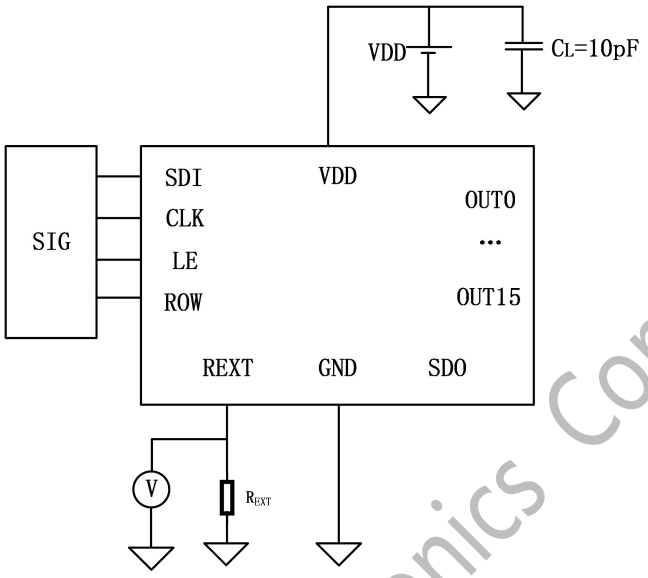
7 Time series waveform diagram



8 Test Circuit Diagram

8.1 TEST Circuit Diagram 1

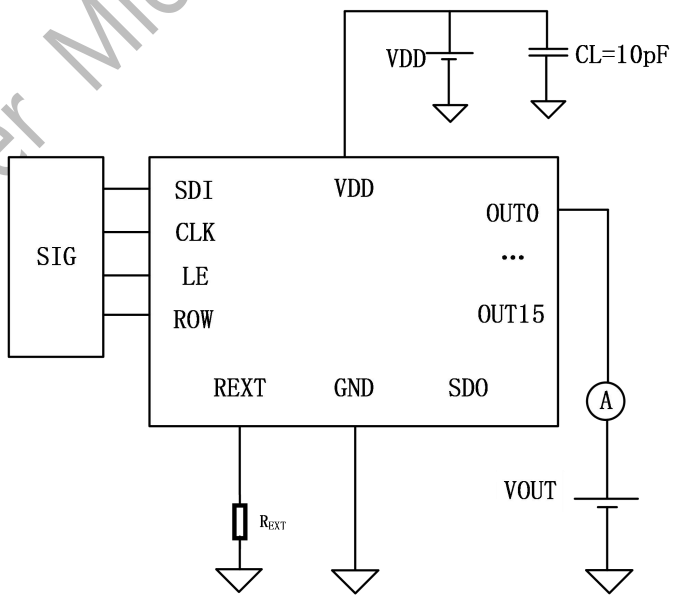
- External resistance and voltage



Test circuit 1 schematic diagram

8.2 TEST Circuit Diagram 2

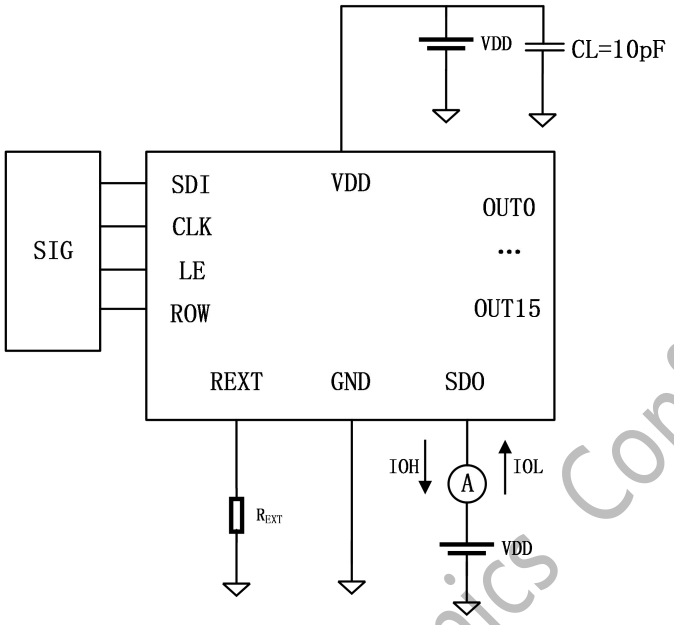
- Constant current output inflection point voltage & corresponding inflection point current (under open circuit detection)



Test circuit 2 schematic diagram

8.3 TEST Circuit Diagram 3

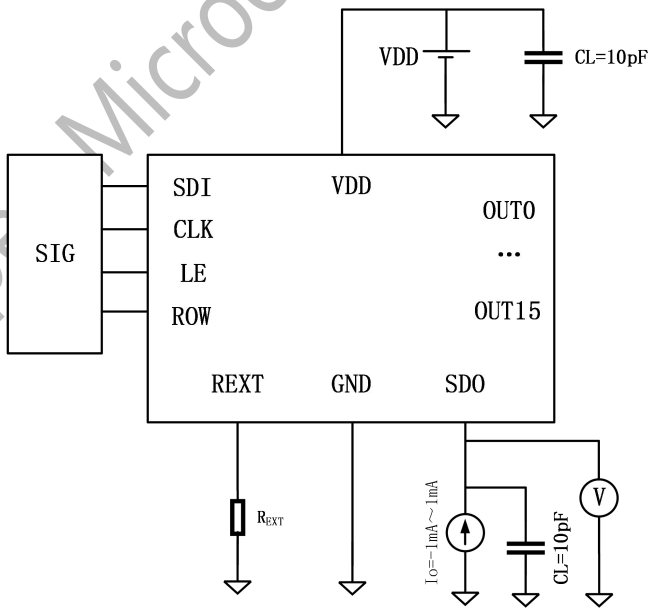
- IOH、IOL



Test circuit 3 schematic diagram

8.4 TEST Circuit Diagram 4

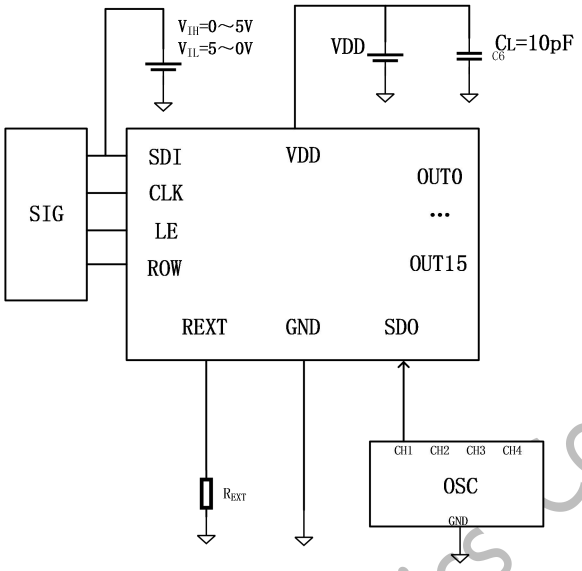
- VOH、VOL



Test circuit 4 schematic diagram

8.5 TEST Circuit Diagram 5

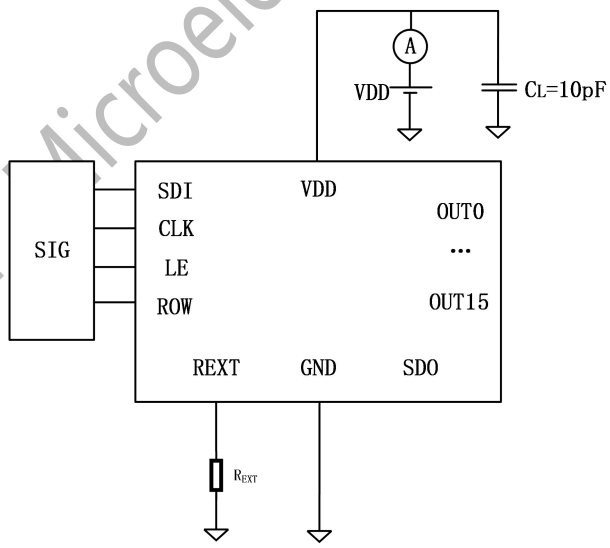
- VIH、VIL



Test circuit 5 schematic diagram

8.6 TEST Circuit Diagram 6

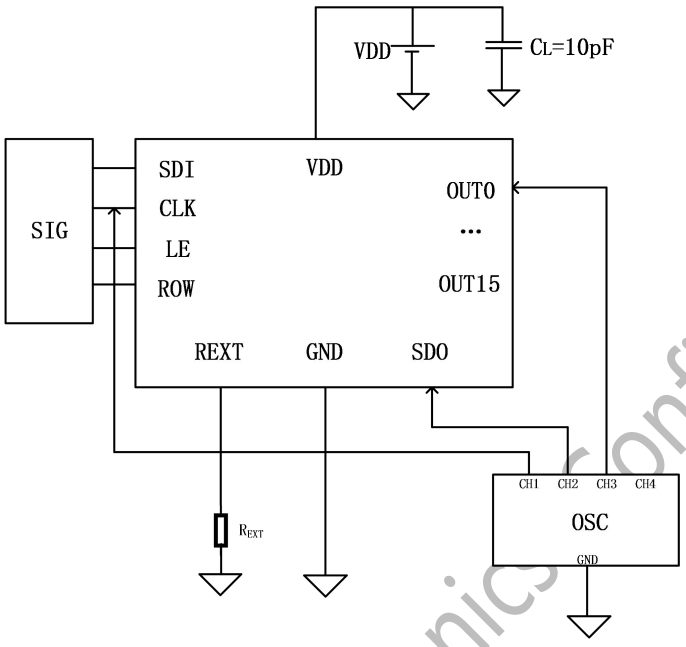
- Power & current



Test circuit 6 schematic diagram

8.7 TEST Circuit Diagram 7

- Dynamic Characteristic



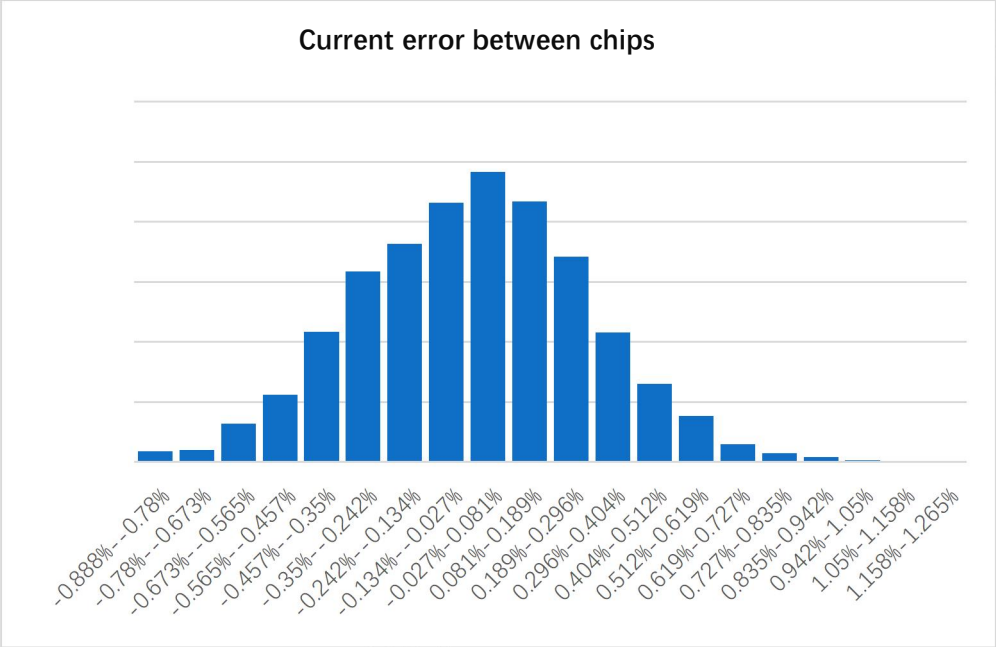
Test circuit 7 schematic diagram

9 Typical Characteristic Diagram

9.1 Constant Current Source Accuracy Test Chart

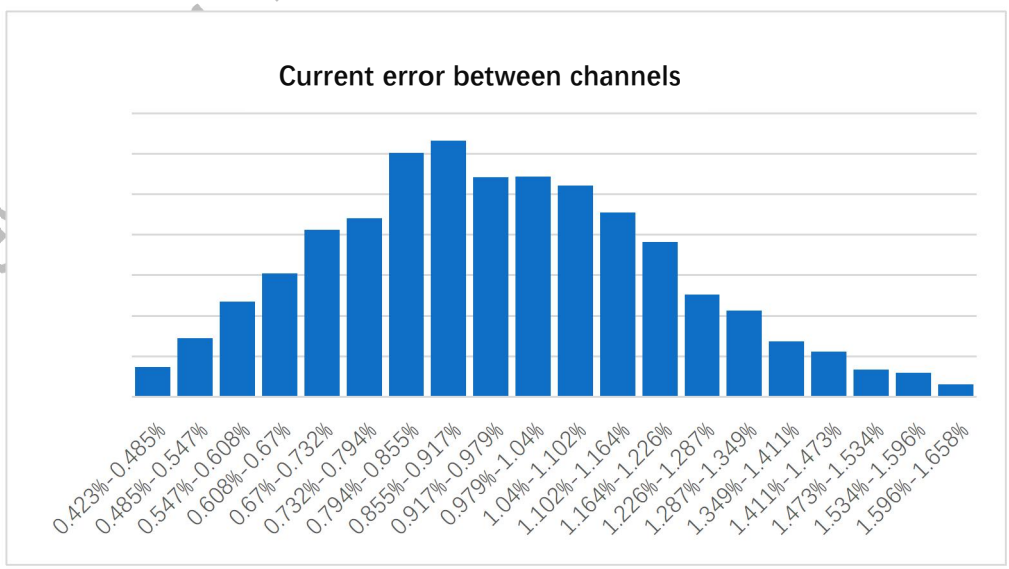
9.1.1 Inter-chip Current Error

Inter-channel current error=$\frac{\text{Average channel current} - \text{average of all chip channels}}{\text{Average of all chip channels}}$



9.1.2 Inter- channel Current Error

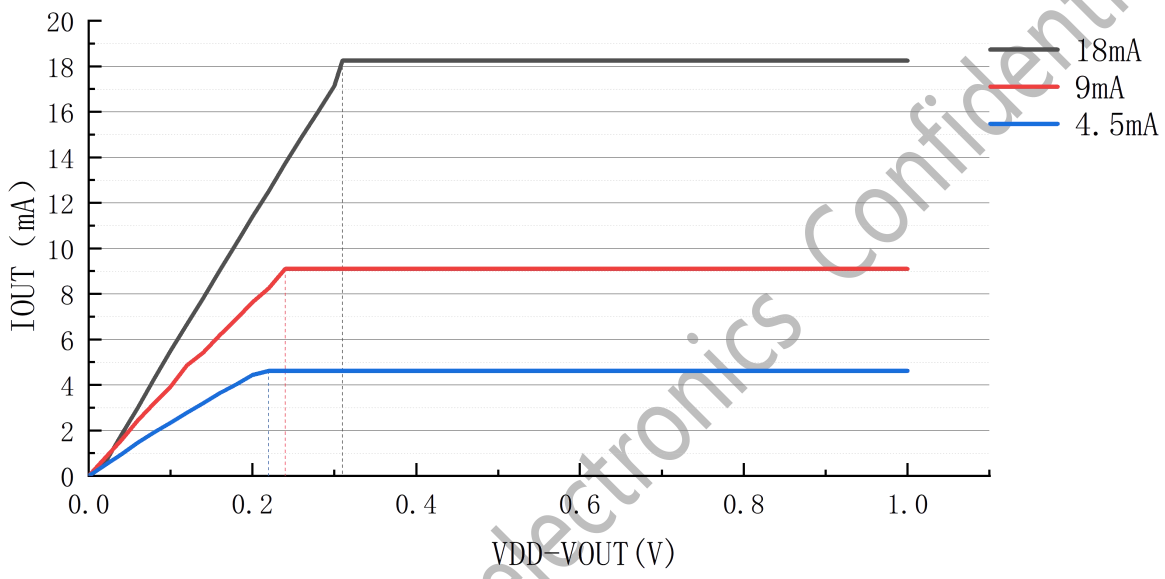
Current error between channels =$\frac{\text{Imax}-\text{Imin}}{\text{Imax}+\text{Imin}}$



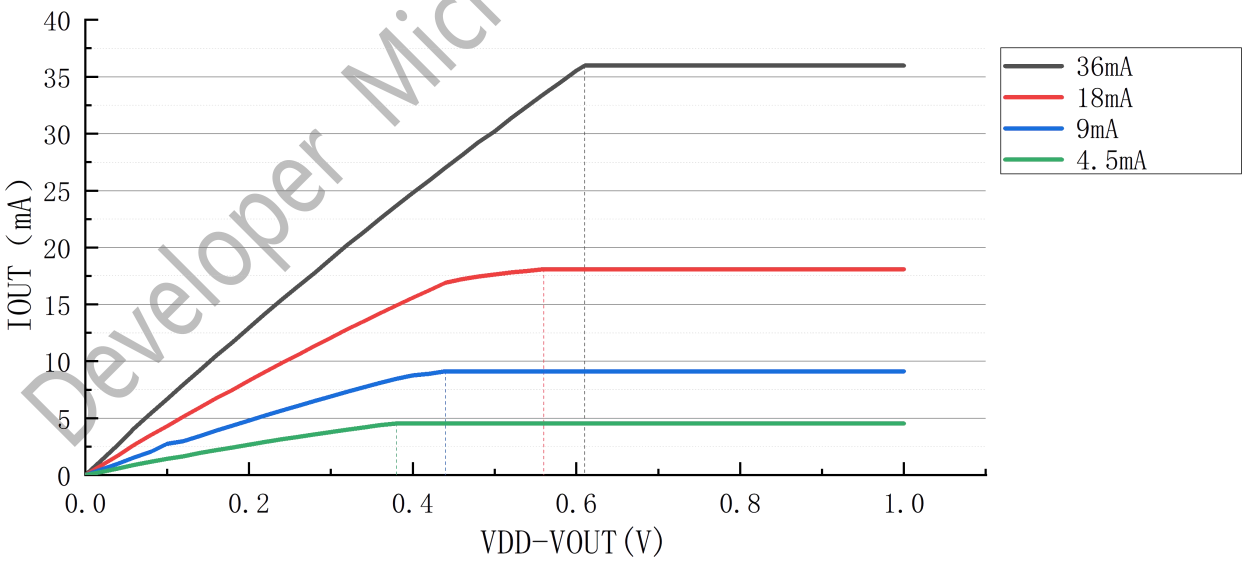
9.2 Constant Current Source Inflection Point

When the DP3269S is applied to the design of LED displays, the current differences between channels and even between chips are minimal. This is due to the DP3269S's excellent constant current output characteristics::

- The maximum on-chip channel current is less than ±2%, and the maximum on-chip current error is less than ±1.5%;
- When the load terminal voltage (V_out) changes, the stability of the output current is not affected, as shown in the figure below:



This is the relation curve between I_OUT and V_OUT when VDD=5V and low Turning point.



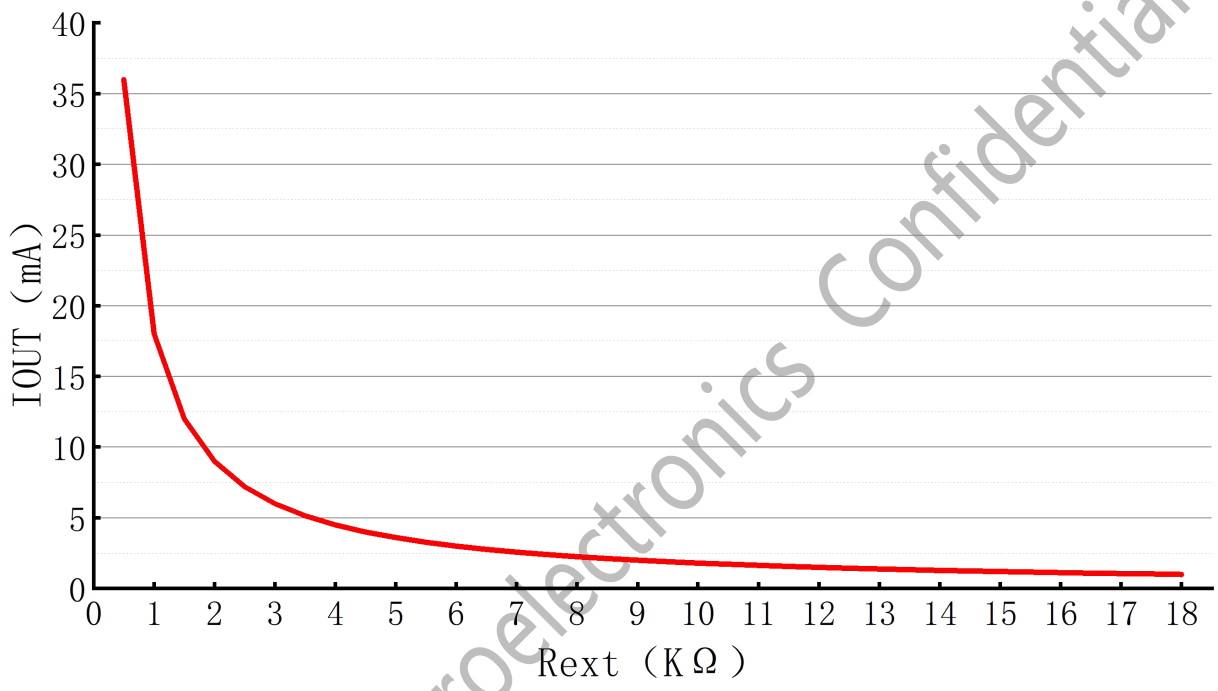
This is the relation curve between I_OUT and V_OUT when VDD=5V and Non- low Turning point.

9.3 Adjust Output Current by An External Resistance

Output current value is calculated by the following formula:

$$\mathbf{IOUT} = \frac{IGAIN*18}{Rext}\mathbf{,\ 12.5\% \le IGAIN \le 200\%}$$

The REXT in the formula is the resistance jointing the ground and the chip's 23PIN REXT port. For example, when the current gain IGAIN=100%, REXT=1kΩ, the output current value can be obtained by calculating the formula 18mA.



IGAIN=100%, the relationship between REXT and I_out

10 Typical Display Effect Sample Image

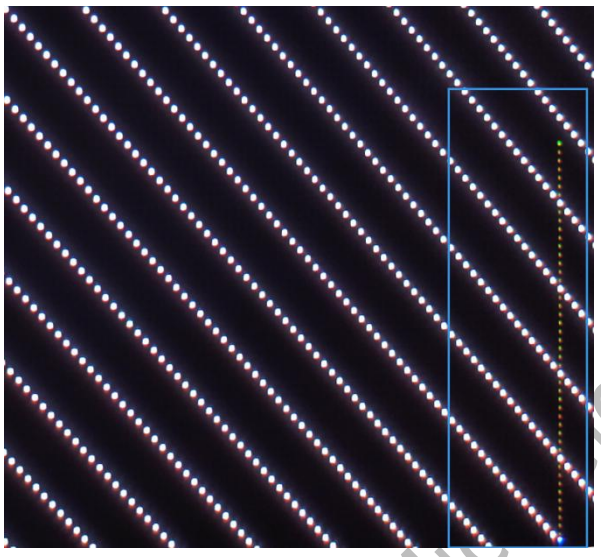
- The specific display effect will be affected by the conditions of the lamp board and register parameters. The following test results are for reference only.

10.1 Display Effect

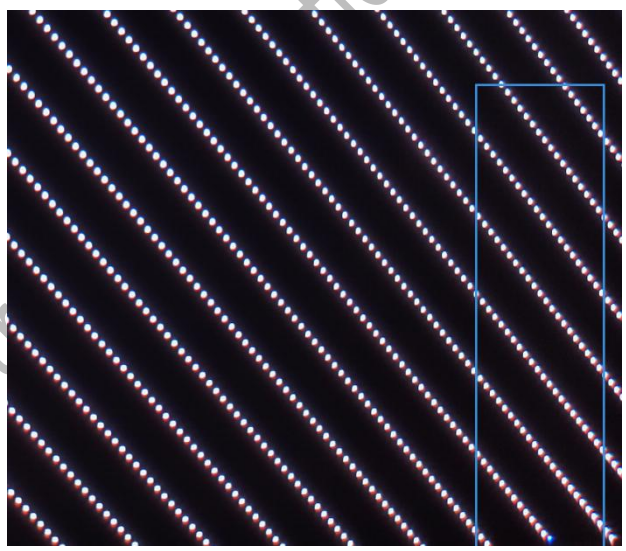
10.1.1 Remove Open Circuit Bad Spot Crosses

The following is a comparison of the display effect before and after removing the open circuit bad spot cross, you can see:

● Chip can remove the bad cross well after removing the open bad cross function, optimize the display effect.



Display Effect before Removing open circuit bad spots cross

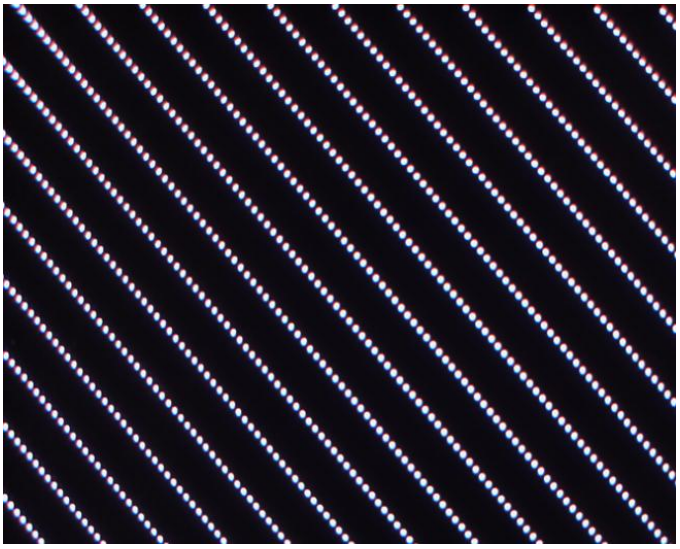


Display effect after removing the open circuit bad spot cross

10.1.2 Remove Ghost and Coupling brightening Effects

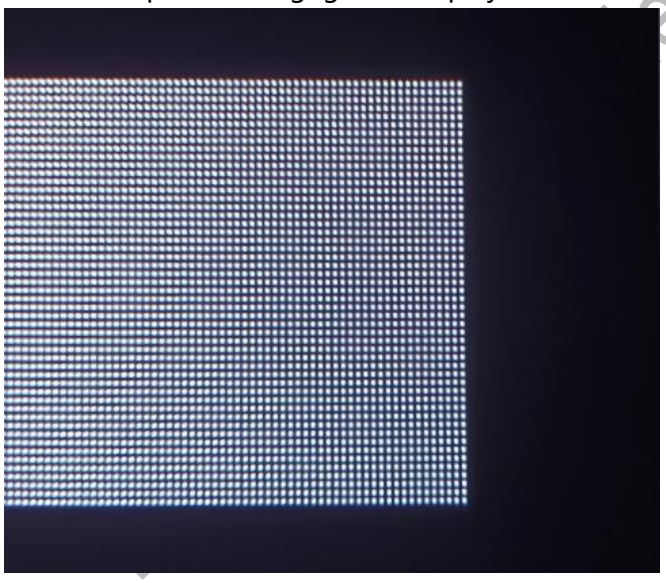
Below is the removal of ghosting and band lighting effect that can be seen:

- Oblique scanning ghost, text ghost and other problems cannot be observed.
- Highlight block with bright, oblique scan superimposed highlight block with bright test results are very good.
- Chip shows good display effect.

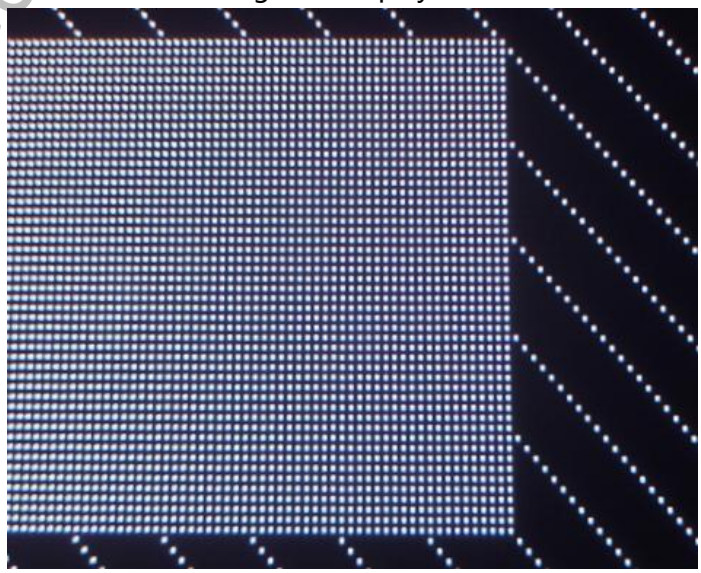


Oblique scanning ghost display effect

Text ghost display effect



White block effect in black display



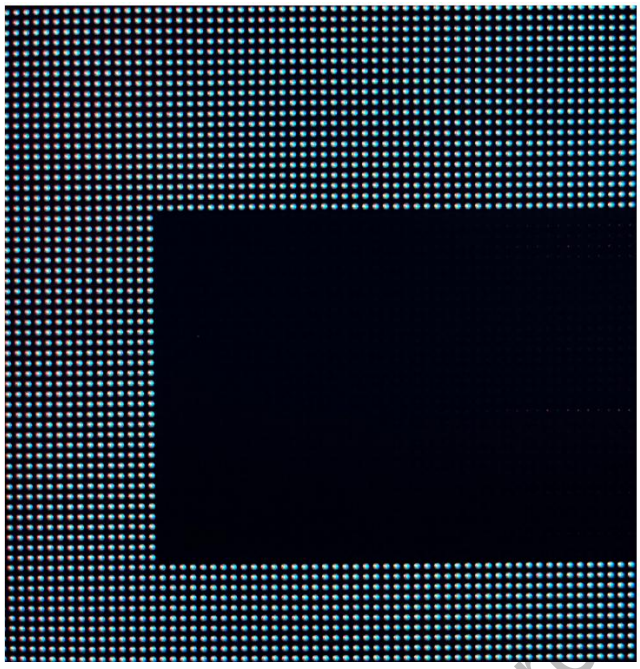
White block effect in Oblique scanning

10.1.3 High and Low Gray Interference and Coupling Display Bad

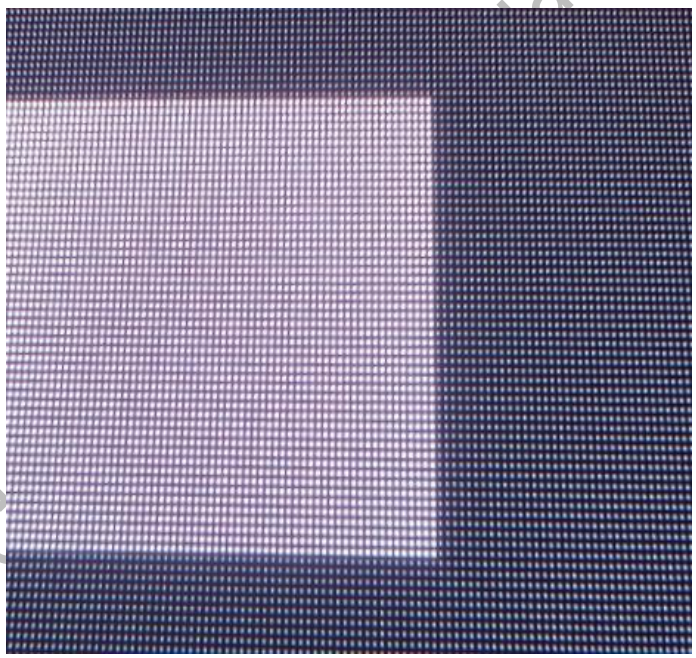
Effect Optimization

The following figure is the optimization effect of high-low gray interference and coupling display poor effects can be seen:

- The low gray coupling of the block and the low gray coupling of the white block are not sensed.
- Chip show good display effect.



Black block effect on low gray scale



White block effect on low gray scale

11 Instruction and Register

11.1 Register Instruction

Instruction Name	Description
DATA_LATCH	Latch 16bit data to SRAM
VSYNC	Enter Double-edge Mode
WR_CFG	Update Display Data
PRE_ACT	Write Register

11.2 Data Instructions

Data sending Sequence	Line	channels
1	Line 0	Channel 15 (OUT15)
2		Channel 14 (OUT14)
.....		.....
16		Channel 0 (OUT0)
17	Line 1	Channel 15 (OUT15)
18		Channel 14 (OUT14)
.....		.....
32		Channel 0 (OUT0)
.....		
1009	Line 63	Channel 15 (OUT15)
1010		Channel 14 (OUT14)
.....		.....
1024		Channel 0 (OUT0)

11.3 Write register

Send PRE_ACT first, then run WR_CFG, LE is 5 DCLK width, the first input 8bit is the register address bit, the last input 8bit is the data bit of the corresponding register address。

11.4 Register signal Sending Way

As shown in the figure above, the order of sending instructions and data in each frame:

1. Send VSYNC。
2. Send PRE_ACT。
3. Send WR_CFG and write the register configuration. Each frame can only write a register value of one address, and 13 frames complete the refresh of all registers (a total of 13 valid register addresses) to save configuration time.
4. Send DAT_LAT several times to write display data together with SDI.
5. The Displayed data send 16 bits, and the low 14bit data t is valid.

11.5 ROW Signal Sending Way

The DP3269S integrated on-chip GCLK generation circuit changes the OE signal of the universal constant current chip to the ROW signal, using ROW the rising edge of the ROW represents the beginning of a row display, where the high level width of the row has two types, namely:

1.W12: The high-level width of the ROW is 12 DCLK width

2.W4: The high-level width of the ROW is 4 DCLK width

(Due to the frequency division of the output DCLK, the width of OE needs to be doubled on the basis of a single edge)

11.6 Double edge mode

Single /Double edge can be selected in the software interface.

11.7 PWM Display Mode

DP3269s integrated three PWM display modes:

1. Universal frame mode; 2. High-gray data independent refresh synchronous mode;
3. High-gray data independently refreshes asynchronous mode;

High-gray data independently refreshes asynchronous mode can improve the taking photo effect,because it can eliminate the black field between frames in the Universal frame mode .

11.7.1 Universal frame mode

Working mode and related configurations as follow:

1. Configure REG0X0C [7:6] = 0 and set the PWM display mode to Universal Frame Sync Mode
2. The number of DCLK per line is calculated using the Formula
3. The configuration shows the number of data sets, REG0X03[6:0] = refresh rate/frame rate -1(if refresh rate is not equal to 3840 or 7680, use Depp's gamma DLL)
4. After VSYNC, the first Line (Line 0) of Group 1(Group 0)

5. Stop displaying data from the current frame until the next VSYNC comes

11.7.2 High-gray data independent refresh synchronous mode

Working mode and related configurations as follow:

1.setting High-gray data independent refresh synchronous mode;
2.Calculate the DCLK Numbers each line by formula ;
3.Setting display date groups by Universal frame mode;
4.Ceaseless Sending the row signal with Fixed display frequency , the frequency has no relationship with VSYNC signal.

11.7.3 High-gray data Independently Refreshes Asynchronous Mode

Working mode and related configurations as follow:

1.Setting High-gray data independently refreshes asynchronous mode
2. Calculate the DCLK Numbers each line by formula
3.Manual Setting display date group by Universal frame mode , default value of the group number is 64. Chip supply the max value is 64.
4.Ceaseless Sending the row signal with Fixed display frequency , the frequency has no relationship with VSYNC signal.
5.Send the ROW signal W12 in the 0line of the 0group, others send W4.

Description:

The main difference between High-gray data independently refreshes asynchronous mode and synchronous mode

1. High-gray data independent refresh synchronous mode:
   The number of display data sets is automatically configured based on the display frame time.
2. High-gray data independently refreshes asynchronous mode:
   The number of display data groups can be manually configured

11.8 Register

Register	Register function Name	Register function Description and Default value
0x02		R: 2A G: 2A B: 2A
7:6		Reserved
5:0	LINE_SET<5:0>	Scan Numbers
0x03		R: 3F G: 3F B: 3F
7		Reserved
6:0	GROUP_SET<6:0>	Display Refresh rate
0x04		R: 20 G: 20 B: 20
7		Reserved
6:0	PWM_WIDTH<6:0>	LINE PWM Width
0x05		R: 34 G: 34 B: 34
7:3	DISSHD_TIME_1<3:0>	Elimination moment

2:0	DISSHD_TIME_2<3:0>	Elimination time
0x06		R：42 G：42 B：42
7:3	DECOUP_RAT<4:0>	Coupling Optimization coefficient
2:0	PLL_DIV<2:0>	Frequency coefficient
0x07		R：00 G：00 B：00
7:0	Gamma	Gamma adjust
0x08		R：7F G：7F B：7F
7:0	IGAIN<7:0>	Current gain
0x09		R：60 G：60 B：60
7:4		Reserved
4:0	DECOUP_1<4:0>	Coupling Optimization 1
0x0a		R：BE G：BE B：BE
7:6	DECOUP_ENHANCE<1:0>	Coupling Optimization enhancement level
5:3		Reserved
2:1	PIT_OPT<1:0>	Low gray spot Optimization
0		Reserved
0x0b		R：28 G：30 B：31
7:5	CORNER <2:0>	Constant current output Grade of inflection point
4:0	DISSHD_LEVEL<4:0>	Extinction level
0x0c		R：90 G：90 B：90
7:6	SYNC_MODE<1:0>	Display mode
5:4	LP_MODE<1:0>	energy-saving mode
3:0		Reserved
0x0d		R：08 G：12 B：18
7:5		Reserved
4:0	DECOUP_LEVEL<4:0>	Coupling optimization level
0x0e		R：48 G：52 B：58
7:0		Reserved
0x0f		R：00 G：00 B：00
7:0		Reserved
0x10		R：00 G：00 B：00
7:0		Reserved
0x11		R：00 G：00 B：00
7:0		Reserved
6:0		Reserved
0x12		R：00 G：00 B：00
7:0		Reserved
0x13		R：00 G：00 B：00
7:0		Reserved
0x14		R：00 G：00 B：00
7:0		Reserved
0x15		R：00 G：00 B：00

7:0		Reserved
0x16		R：00 G：00 B：00
7:0		Reserved
0x17		R：00 G：00 B：00
7:0		Reserved

12 Encapsulation Cooling Power (PD)

The maximum heat dissipation power of the encapsulation is determined by the formula: $P_{D(\max)} = \frac{(T_j - T_a)}{R_{th(j-a)}}$

When all 16 channels are open, the actual power is:

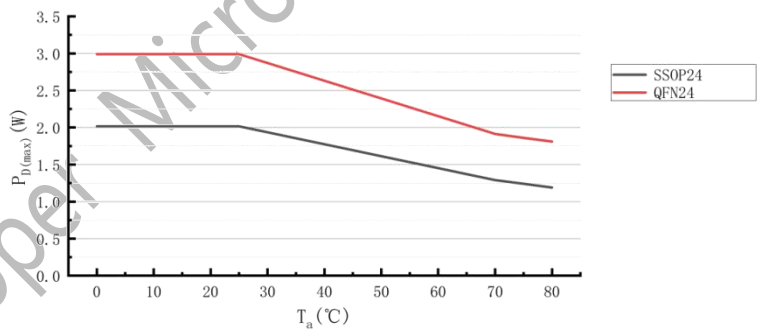
$P_{D(act)} = I_{DD} * V_{DD} + I_{OUT} * Duty * V_{DS} * 16$

To ensure that $P_{D(act)} \le P_{D(max)}$ output maximum current and duty cycle relationship is:

$$I_{OUT(max)} = \frac{\frac{T_j - T_a}{R_{th(j-a)}} - (I_{DD} * V_{DD})}{V_{DS} * Duty * 16}$$

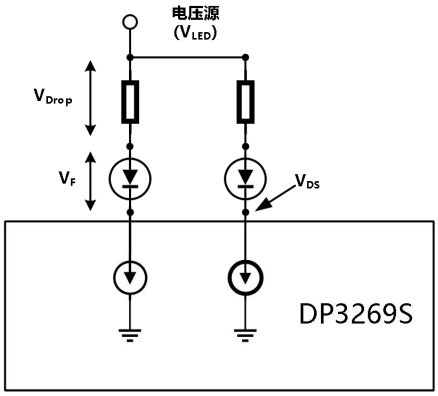
Therein T_j is the junction temperature (T_j=150℃), T_a is the ambient temperature, V_{DS} is the constant current output port voltage, Duty is the duty cycle, and $R_{th(j-a)}$ is the thermal resistance of the encapsulation.

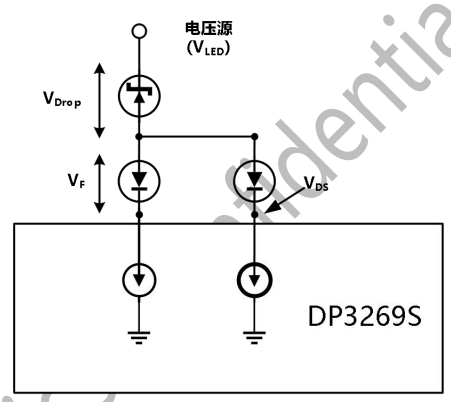
Package	$R_{th(j-a)}$(℃/W)	$P_{D(max)}$(W)
QSOP24	62	2.01
QFN24	41.8	2.99



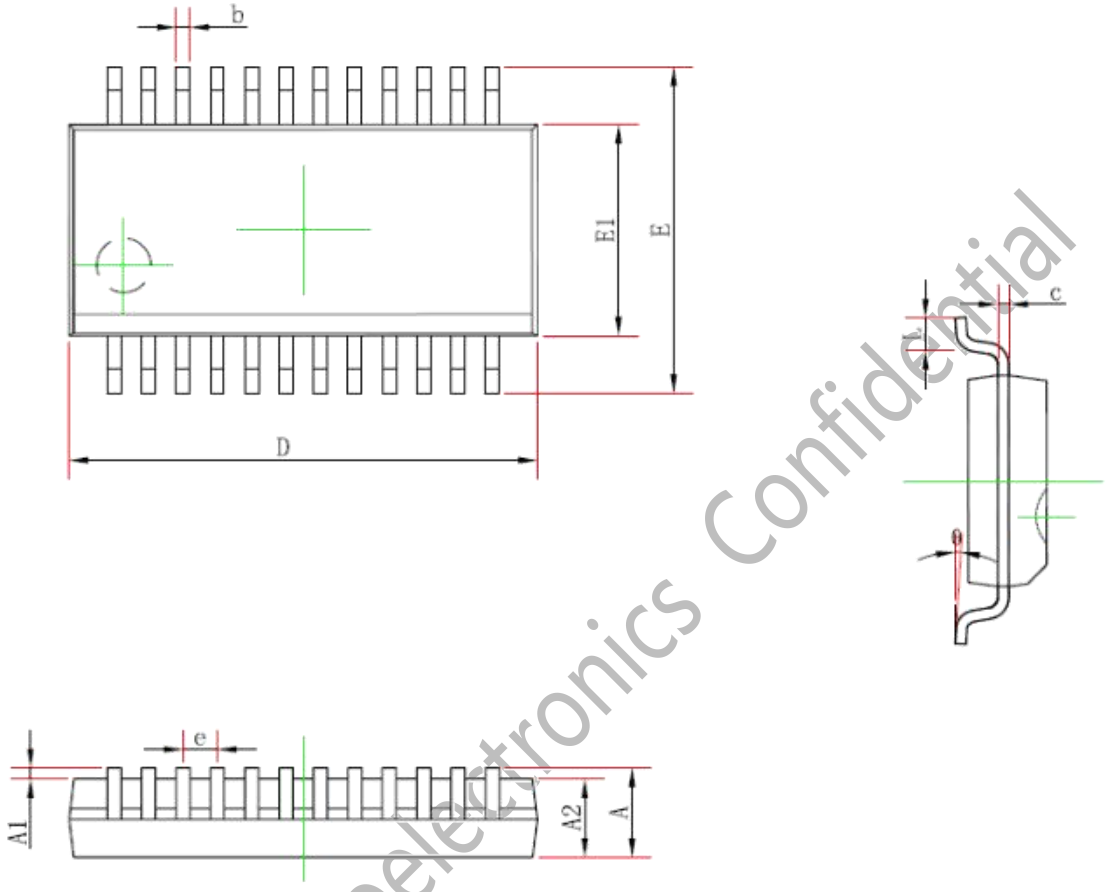
13 Load Terminal Voltage(VLED)

In order to optimize the heat dissipation capacity of the package, it is recommended that the best operating range of the output terminal voltage (VDS) is 0.3V to 1.0V(IOUT= 0.5-36mA). If VDS=VLED-VF and VLED=5V, the high output voltage (VDS) may cause PD (act) > PD (max); In this case, it is recommended to use the lowest possible VLED voltage for use, and an external resistor or voltage regulator can also be used as a VDROP. This results in VDS=(VLED-VF)-VDROP, which reduces the input voltage (VDS) value. The application diagram of the external series resistor or voltage regulator can be referred to the following figure.



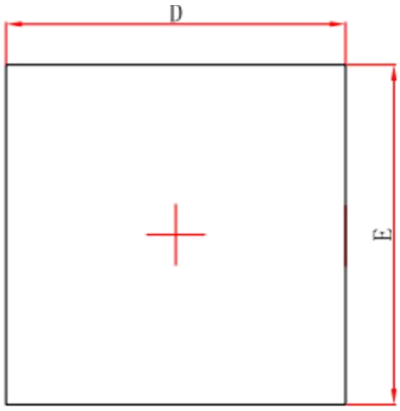


14 Encapsulation Information

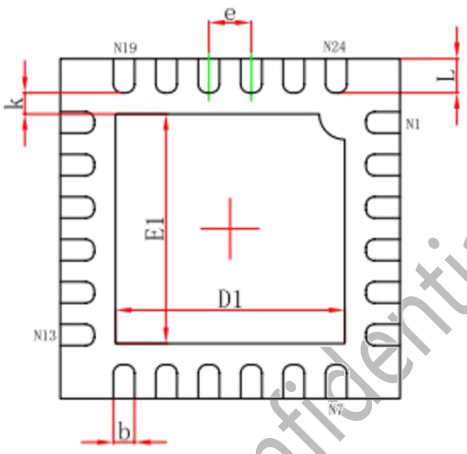


	(mm)	
	(Min)	(Max)
A	—	1.95
A1	0.05	0.35
A2	1.05	—
b	0.1	0.4
c	0.05	0.254
D	8.2	9.2
E1	3.6	4.2
E	5.6	6.5
e	0.635TYP	
L	0.3	1.5
θ	0°	10°

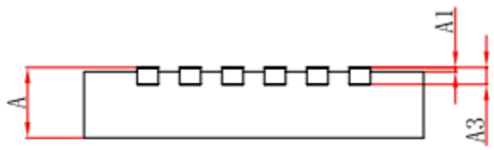
- QSOP24 Plastic Encapsulation Specification Drawing



Top View



Bottom View



Side View

	(mm)	
	(Min)	(Max)
A	0.700/0.800	0.800/0.900
A1	0.000	0.050
A3	0.203REF	
D	3.924	4.076
E	3.924	4.076
D1	2.6	2.8
E1	2.6	2.8
k	0.20MIN	
b	0.200	0.300
e	0.500TYP	
L	0.324	0.476

15 Official Announcement

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