DP3369S Common Cathode 16-channel PWM Constant Current Source Driver

1 Overview

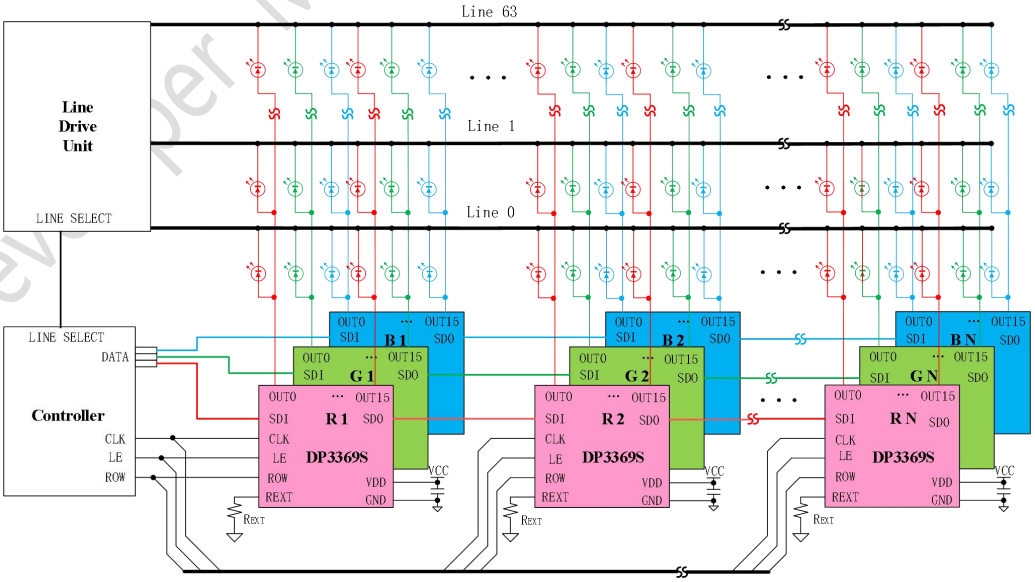
DP3369S is a low-latency PWM constant current source driver chip specifically designed for LED display screens. The chip supports up to 16-bit grayscale levels, and integrates high-precision current generation circuitry, allowing the current deviation between chips to be controlled within 2.0%. Additionally, it incorporates multiple exclusive technologies aimed at enhancing the display effect of LED screens, providing significant improvements to the display quality.

2 Features

- Power supply voltage range: 2.6V~5.5V
- Operating temperature range: -40℃ ~85℃
- Scan range: 1~64 scan, any adjustable
- 16 constant current output channels
- Support for no external resistance mode
- Constant flow output range
  - 0.5mA ~ 18mA (V_{out}=0.3V)
  - 0.5mA ~ 25mA (V_{out}=0.6V)
- Inter-channel current error
  - Typical value: ± 1.0% Max value: ± 2.0%
- Inter-chip current error
  - Typical value: ± 0.2% Maximum value: ± 2.0%
- The highest refresh rate supports 128 times the frame rate
- High ash independent refresh, no black field between frames
- Optimize the display status
  - Improve the low-ash uniformity
  - Improve the first line of partial darkness phenomenon
  - Improve the phenomenon of the ghost shadows
  - Improve the high and low grey coupling
  - Improve cross-plate coupling
- Integrated PLL produces in-house GCLK with a lower EMI
- Packaging form: QSOP24 / QFN 24

3 Application area

- High refresh rate LED video display
- Full-color LED display
- High-density small-spacing LED light board display



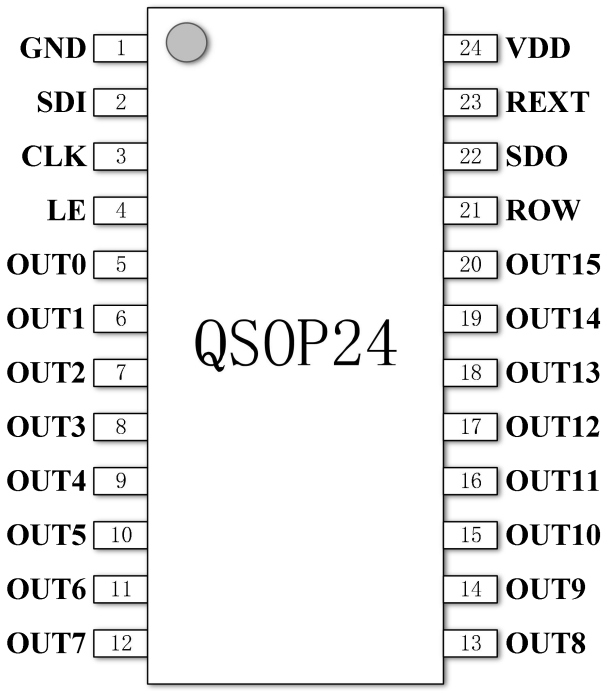
DP3369S A Schematic diagram of the typical application

Catalogue

Revise the history

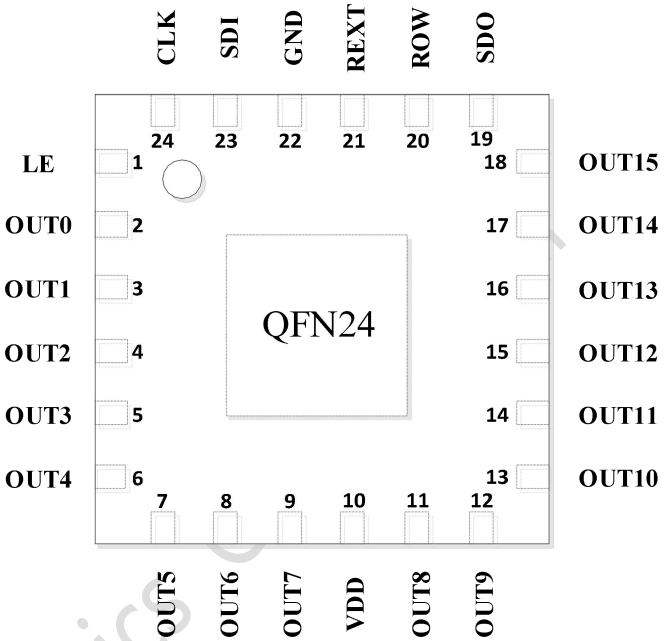
edition	Revised date	Revised	Revised content
V1.0	2024.03	Wang Mei	The initial version
V1.1	2024.04	Wang Mei	1. Optimize the content of the electrical parameters 2. New non-low turning point inflection point chart 3. Add a constant current accuracy test diagram

4 Product description



QSOP24 Pin definition diagram

- The pin definition



The QFN 24 pin definition diagram

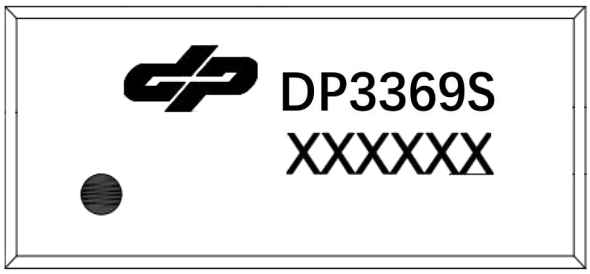
- Feet instructions

QSOP24 Pin number	The QFN 24 pin number	Feet name	Feet instructions
1	22	GND	Chip ground end
2	23	SDI	Serial data input side
3	24	CLK	Serial clock input end
4	1	LE	The latch end of the data and instructions, and different LE lengths represent different instructions
5 ~ 20	2 ~ 9 11 ~ 18	OUT0 ~ OUT15	Constant flow output
21	20	ROW	Change the line signal
22	19	SDO	Serial data output side
23	21	REXT	Connect external resistance
24	10	VDD	Chip power end

- Product order information

product name	Packaging form	manner of packing	Quantity / plate	Wet sensitivity level
DP3369S	QSOP24	braid	4000	MSL=3
	QFN24	braid	5000	

- Product marking



QSOP24

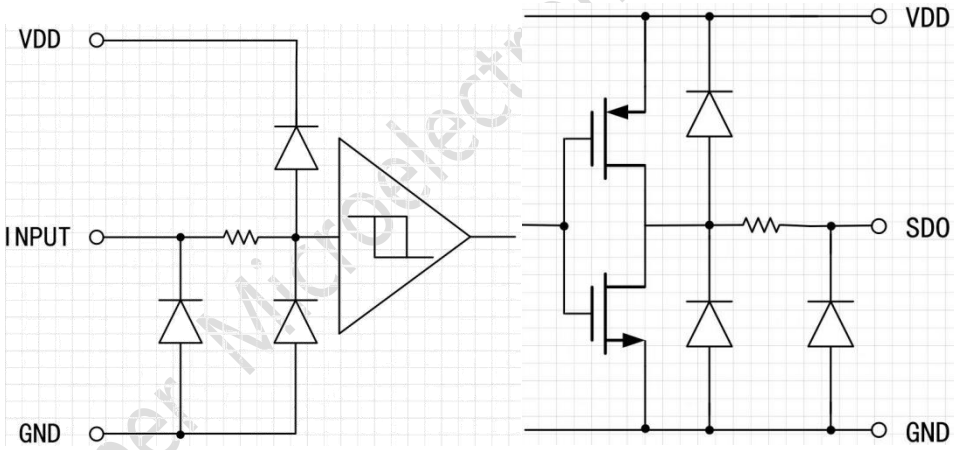
QFN24

DP3369S The name of the product
XXXXXX Represents the product lot number

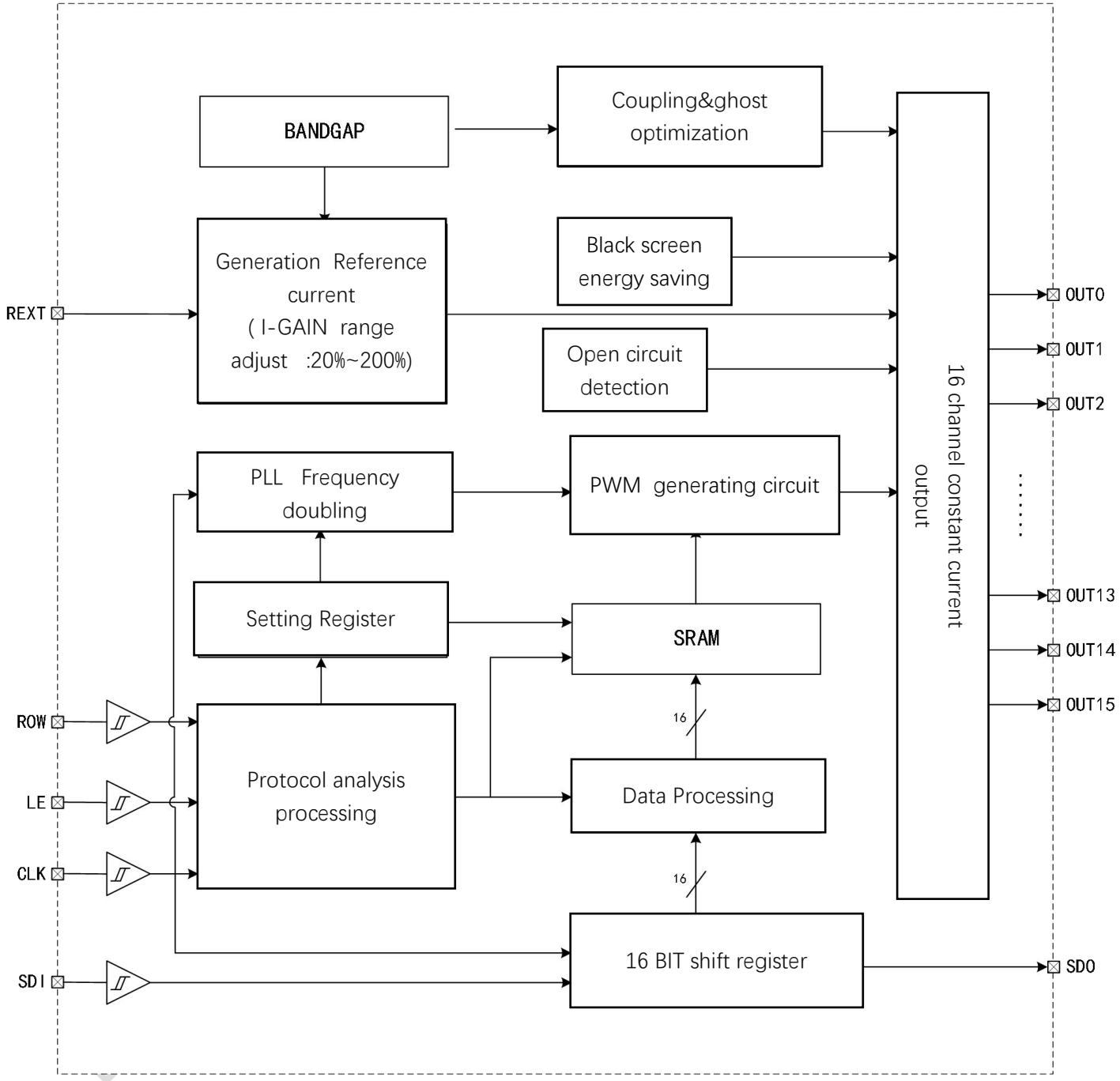
5 Circuit schematic diagram

5.1 Input-output equivalent circuit

SDI, CLK, LE, OE input end SDO output end



5.2 Internal circuit block diagram



A Schematic diagram of the internal circuit

6 Parameter list

6.1 Maximum limit parameter

project	symbol	rating	unit
supply voltage	V_{DD}	0 ~ 6	V
output	I_O	25	mA
input voltage	V_{IN}	-0.4 ~ V_{DD}+0.4	V
Output tolerance voltage	V_{OUT}	11	V
clock frequency	F_{CLK}	25	MHz
working temperature	T_{opr}	-40 ~ 85	℃
Storage temperature	T_{stg}	-55 ~ 150	℃

- All the voltage values are based on the chip ground end (GND) as the reference point, and the test temperature of the maximum limit parameter is 25℃.
- The actual working conditions exceeding the specified value may cause permanent damage to the components; the actual working conditions falling slightly below the maximum value and working for long hours may reduce the reliability of the components. The above is only partially specified values, and this product does not support functional operation under other conditions than the specification.
- The highest welding temperature of the table paste product shall not exceed 260℃. The temperature curve shall be set by the factory according to the J-STD-020 standard, refer to the actual factory and the manufacturer of the tin paste.

6.2 ESD grade

6.2.1 Contact ESD

symbol	condition		least value	representative value	crest value	unit
$V_{(ESD)}$	Human Discharge Model (HBM)[1]	OUTn Pin-GND	-	±8	-	kV
		OTHER Pin-GND	-	±8	-	kV
	machine model (MM)[2]	OUTn Pin-GND	-	±0.4	-	kV
		OTHER Pin-GND	-	±0.4	-	kV

- [1] The lowest HBM model ESD voltage of all the pins meets the Class-3B standard in the JEDEC JS-001-2017 file.
- [2] The lowest MM model ESD voltage of all pins meets the Class-C standard for the JEDEC EIA / JESD22-A115C file.

6.3 Electrical characteristics (VDD=3.5V~5V, Ta=25℃)

project	symbol	test circuit	test condition		least value	representative value	crest value	unit
REXT voltage characteristic	VR_TT	1	V_{DD}=5V,R_{EXT}=1K IGAIN=100%,T_a=25℃			1.498		V
	VR_LT		V_{DD}=5V R_{EXT}=1K IGAIN=100%	T_a=-40℃	-	1.485	-	V
	VR_HT			T_a=85℃	-	1.505	-	V
Constant flow output inflection point	V_{OUT1}	2	V_{DD}=5.0V R_{EXT}=1k Turning point level 0	IOUT=18mA	-	270	-	mV
	V_{OUT2}			IOUT=9mA	-	230	-	mV
	V_{OUT3}			IOUT=4.5mA	-	200	-	mV
	V_{OUT4}		V_{DD}=5.0V R_{EXT}=1k Turning point level 1	IOUT=18mA	-	300	-	mV
	V_{OUT5}			IOUT=9mA	-	250	-	mV
	V_{OUT6}			IOUT=4.5mA	-	230	-	mV
	V_{OUT7}		V_{DD}=5.0V R_{EXT}=1k Turning point level 2	IOUT=18mA	-	330	-	mV
	V_{OUT8}			IOUT=9mA	-	280	-	mV
	V_{OUT9}			IOUT=4.5mA	-	250	-	mV
	V_{OUT10}		V_{DD}=5.0V R_{EXT}=1k Turning point level 3	IOUT=18mA	-	342	-	mV
	V_{OUT11}			IOUT=9mA	-	302	-	mV
	V_{OUT12}			IOUT=4.5mA	-	280	-	mV
	V_{OUT13}		V_{DD}=5.0V R_{EXT}=1k Turning point level 4	IOUT=18mA	-	420	-	mV
	V_{OUT14}			IOUT=9mA	-	382	-	mV
	V_{OUT15}			IOUT=4.5mA	-	360	-	mV
Constant current source output range	IOUT	2	Turning point level 0		0.5	-	18	mA
	IOUT1		Turning point level 1		0.5	-	21	mA
	IOUT2		Turning point level 2		0.5	-	25	mA
	IOUT3		Turning point level 3		0.5	-	25	mA
	IOUT4		Turning point level 4		0.5	-	25	mA
Interchip output current error	DCHIP	2	VDS=0.6V		—	±0.2	± 2.0	%
Interchannel output current error	DCHL	2	VDS=0.6V		—	± 1.0	±2.0	%
Constant current error / VDS, the	%/ΔVDS	2	VDS=0.3~3.0V		—	—	± 1.0	%/V

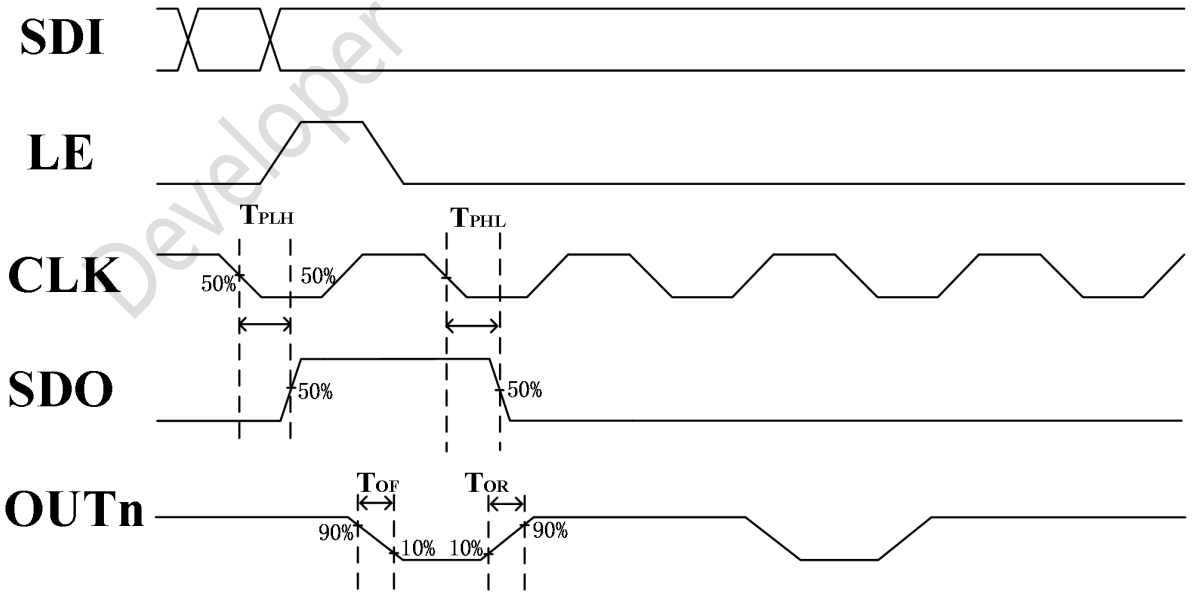
variation amount								
Constant current error / VDD variation		%/Δ VDD	2	VDD=3.5V~5.0V	—	—	± 1.0	%/V
Output voltage at the ON		$V_{O(ON)}$	2	OUT0~OUT15	0.3	-	V_{DD}	V
SDO drive current	high level	IOH	3	VDD=5V	—	-22	—	mA
	low level	IOL			—	23	—	mA
output level	high level	VOH	4	IOH=-1mA	4.6	—	—	V
	low level	VOL		IOL=1mA	—	—	0.4	V
High-level logic input voltage		V_{IH}	5	-	0.7*V_{DD}	-	V_{DD}	V
Low-level logic input voltage		V_{IL}		-	GND	-	0.3*V_{DD}	V
Power supply current / with resistance (White screen power consumption)		I_{DD1}	6	R_{EXT}=3K, white screen, and VDD=2.8V IOUT = 6 mA, with a refresh rate of 3,840	4.63	-	-	mA
Power supply current / with resistance (Black screen energy-saving power consumption)		I_{DD3}	6	R_{EXT}=3K, black screen, VDD=2.8V IOUT = 6 mA, and the performance is preferred	1.8	-	-	mA
		I_{DD4}		R_{EXT}=3K, black screen, VDD=2.8V IOUT = 6 mA, and the low power consumption is preferred	0.84	-	-	mA
		I_{DD5}		R_{EXT}=3K, black screen, VDD=2.8V IOUT = 6 mA, with very low power consumption	0.41	-	-	mA
Power supply current / no resistance (White screen power consumption)		I_{DD1}	6	R_{EXT}=3K, white screen, and VDD=2.8V IOUT = 6 mA, with a refresh rate of 3,840	3.09	-	-	mA
Power supply current / no resistance (Black screen energy-saving power consumption)		I_{DD3}	6	R_{EXT}=3K, black screen, VDD=2.8V IOUT = 6 mA, and the performance is preferred	1.8	-	-	mA
		I_{DD4}		R_{EXT}=3K, black screen, VDD=2.8V IOUT = 6 mA, and the low	0.84	-	-	mA

			power consumption is preferred				
	I_{DD5}		R_{EXT}=3K, black screen, VDD=2.8V IOUT = 6 mA, with very low power consumption	0.41	-	-	mA

6.4 Dynamic characteristics (VDD=3.5V~5V, Ta=25℃)

project	symbol	test circuit	test condition	least value	representative value	crest value	unit
The CLK-SDO delay	TPHL	7	VDD=5V, FDCLK=12.5MHz	-	50	-	ns
The CLK-SDO delay	TPLH			-	50	-	ns
Constant current output rise time	tOR		IOUT=10mA, ΔVOUT=3V	-	45	-	ns
Constant current output drop time	tOF			-	35	-	ns

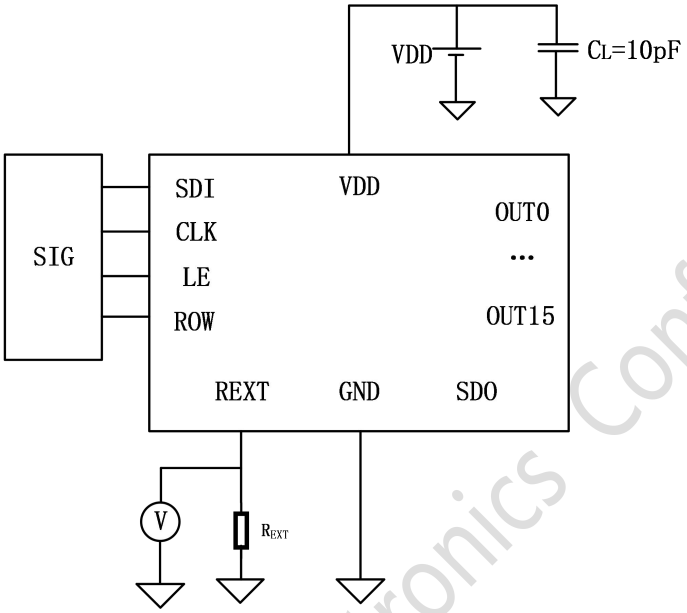
7 Time sequence waveform



8 Test circuit diagrams

8.1 Test circuit 1

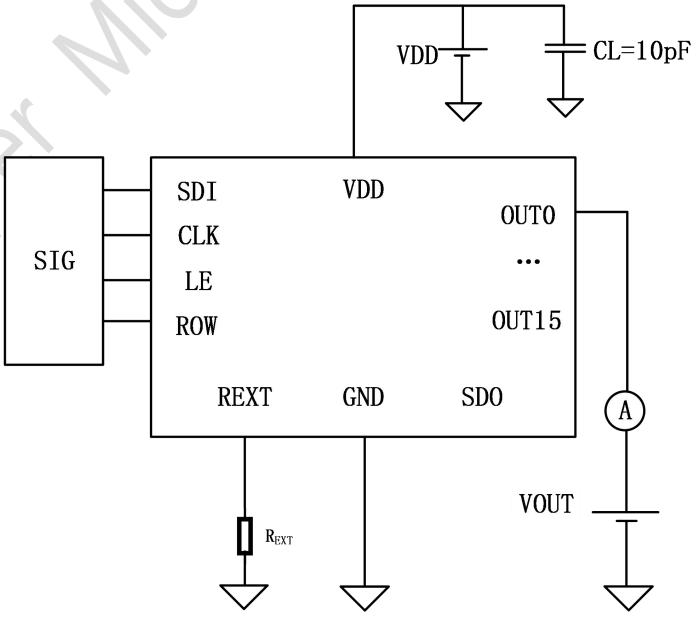
- External resistance voltage



A Schematic diagram of the test circuit 1

8.2 Test circuit 2

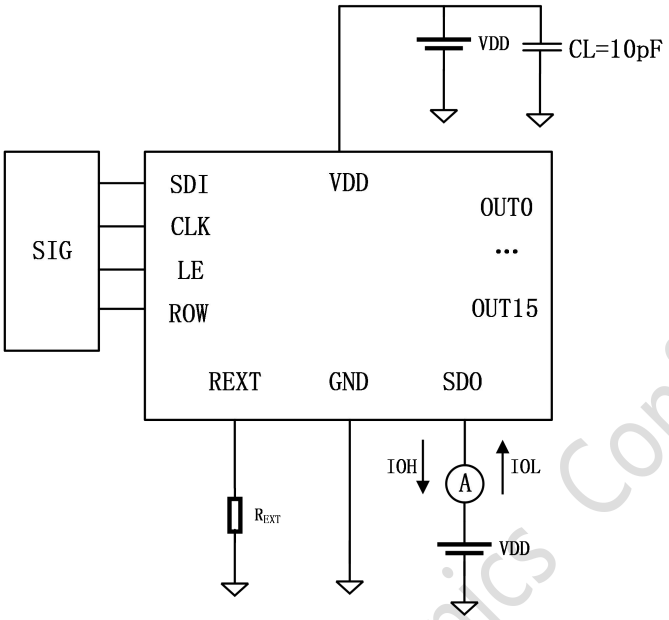
- Constant current output inflection point voltage & corresponding inflection point current (test in open circuit detection state)



A Schematic diagram of the test circuit 2

8.3 Test circuit 3

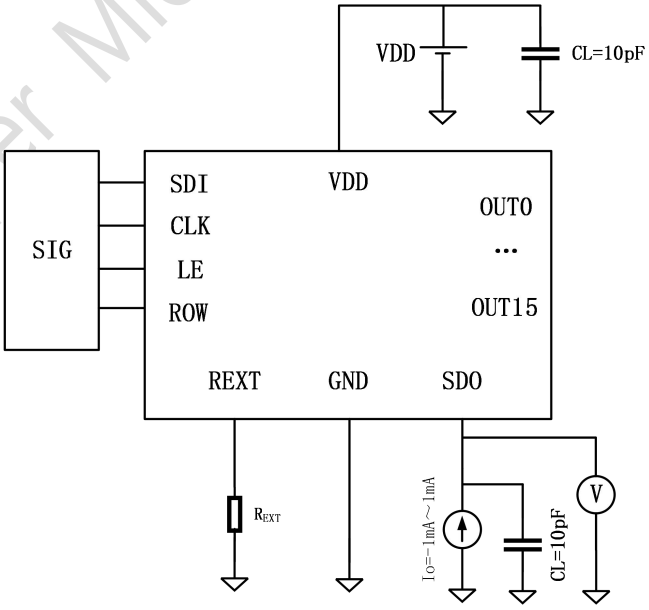
- IOH、IOL



A Schematic diagram of the test circuit 3

8.4 Test circuit 4

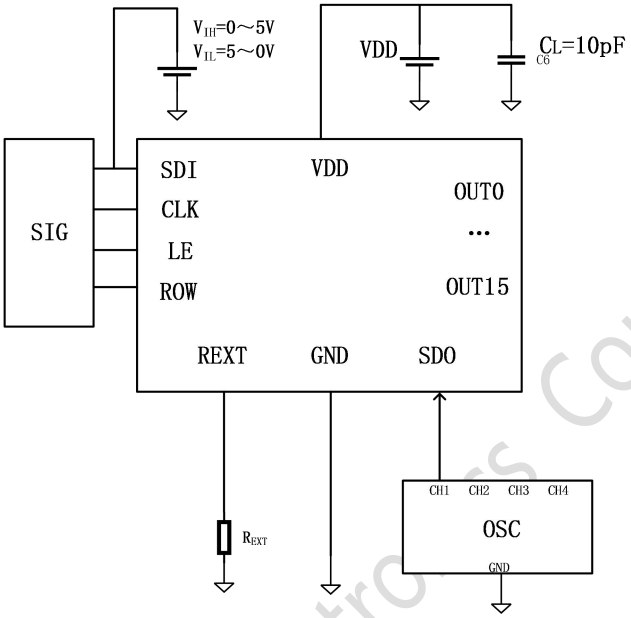
- VOH、VOL



A Schematic diagram of the test circuit 4

8.5 Test circuit 5

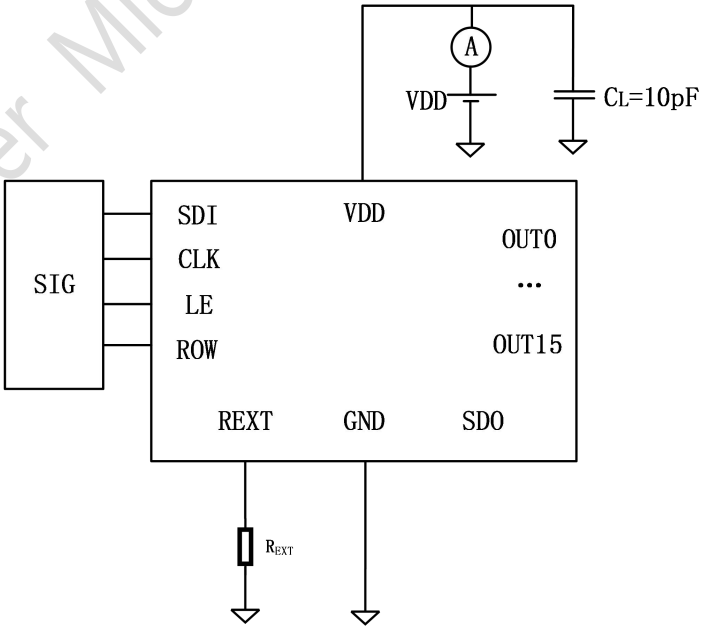
- VIH、VIL



A Schematic diagram of the test circuit 5

8.6 Test circuit 6

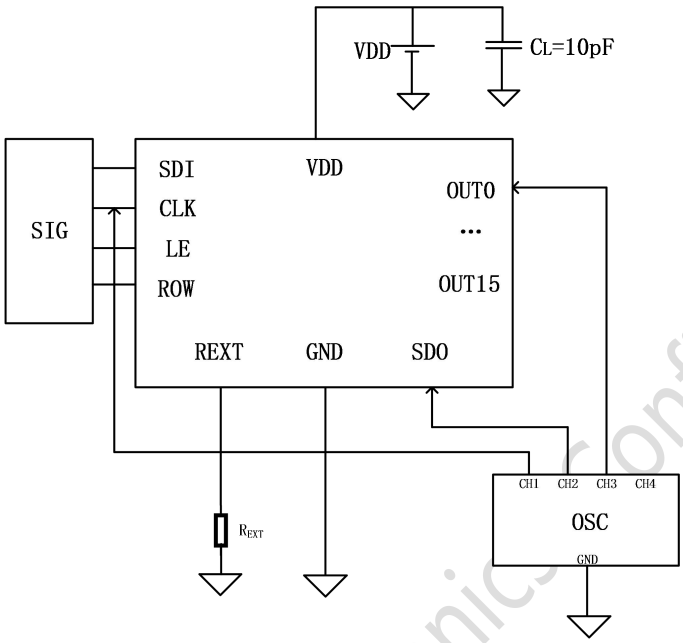
- source current



A Schematic diagram of the test circuit 6

8.7 Test circuit 7

- dynamic characteristis

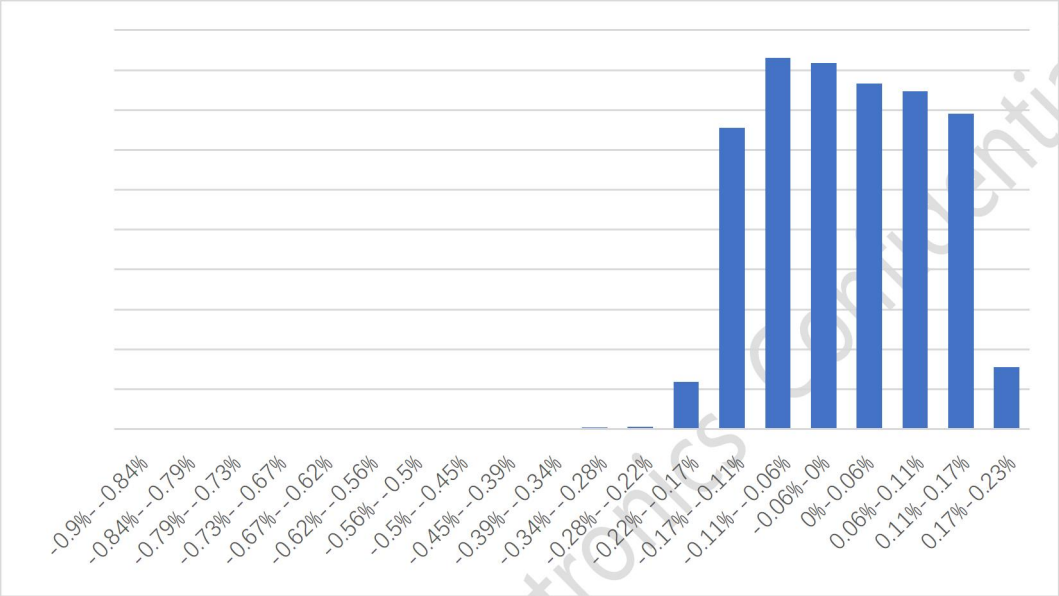


A Schematic diagram of the test circuit 7

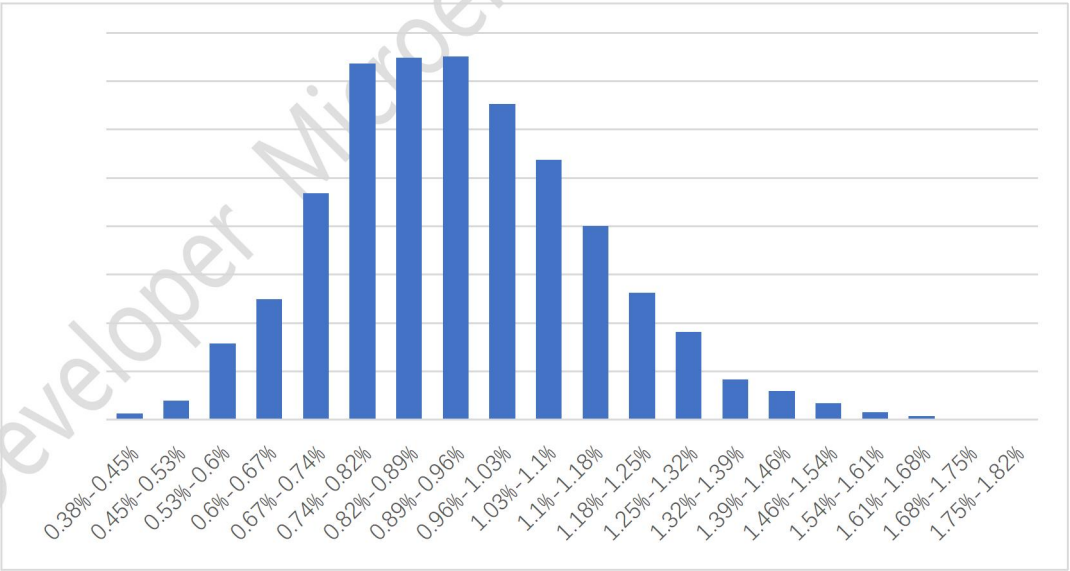
9 Typical feature diagram

9.1 Constant current source accuracy test chart

9.1.1 Inter-chip current error



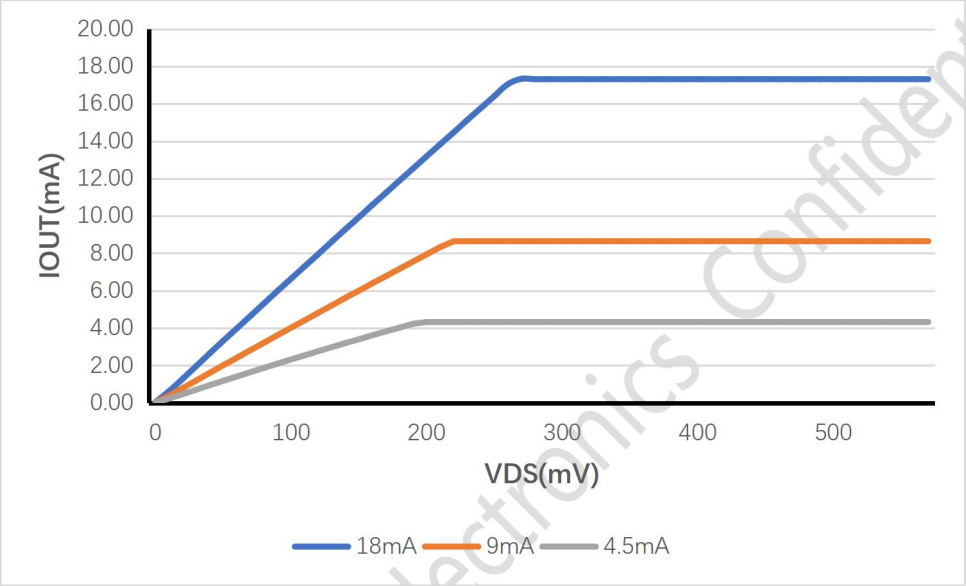
9.1.2 Inter-channel current error



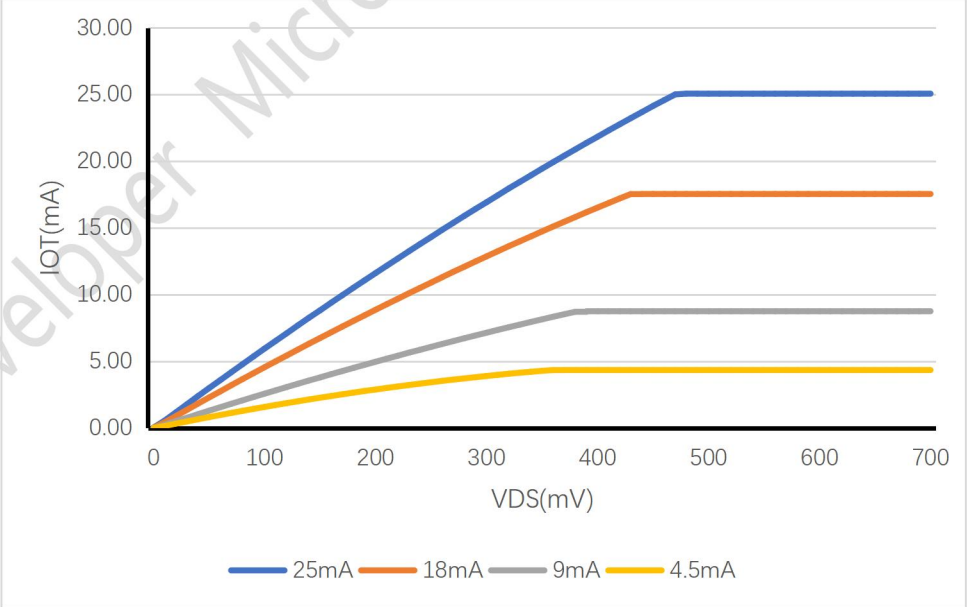
9.2 Constant flow source inflection point

When applying DP3369S to LED display design, the current difference between channels and even between chips is minimal. This is derived from the excellent constant current output characteristics of the DP3369S:

- The maximum current between the chip channels is less than ± 2.0%, while the maximum current error between the chips is less than ± 2.0%;
- When the load end voltage (V out) changes, the stability of the output current is not affected, as shown in the figure below:



The relationship curve between IOUT and VOUT in low turning mode, VDD = 5 V



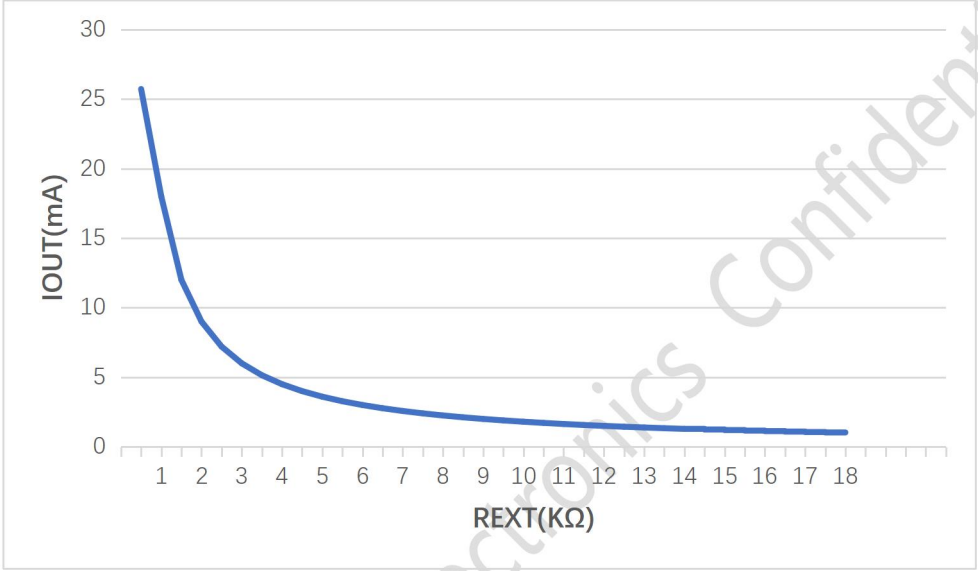
The relationship curve between IOUT and VOUT, VDD = 5 V

9.3 Adjust the output current by using the external resistance

The output current value is calculated as follows:

$$IOUT = \frac{IGAIN*18}{Rext}, \ 12.5\% \ \ IGAIN \ \ 200\% \leq\leq$$

R in formula$_{EXT}$Is the ground-to-ground resistance value of the 23PIN REXT port of the chip. For example, when the current gain IGAIN = 100%, R_{EXT}At = 1 kΩ, the output current value of 18 mA can be obtained by calculating the formula.



IGAIN=100%，R_{EXT}The relationship curve with Iout

10 Typical display effect pattern

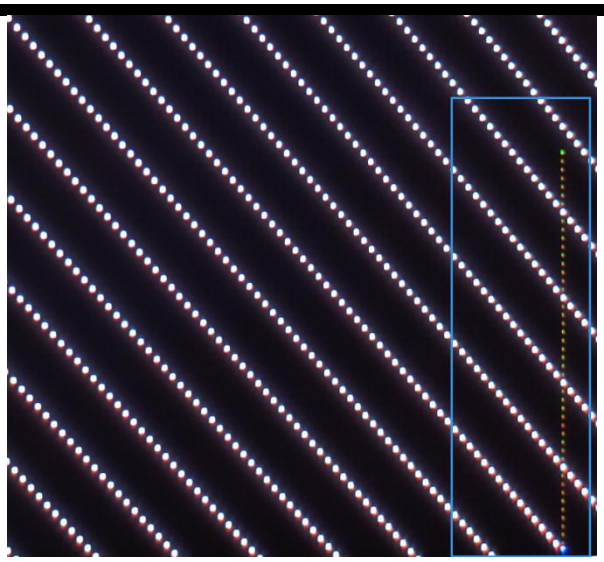
- The specific display effect will be affected by the lamp plate conditions and register parameters, and the following test results are only of reference significance.

10.1 Display effect

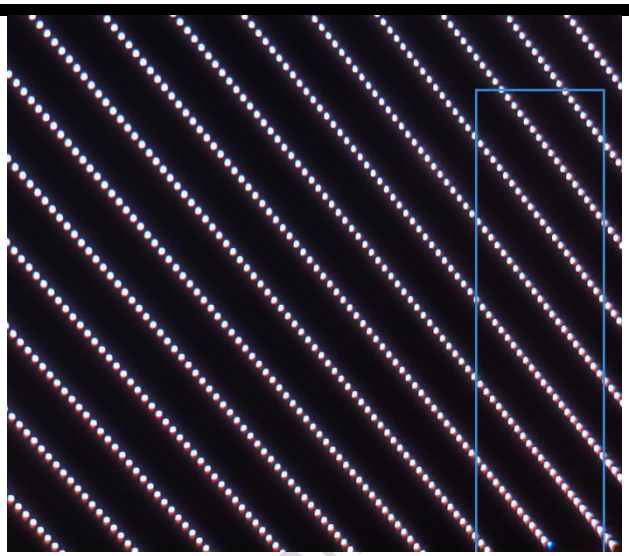
10.1.1 Remove the open circuit break point cross

The following is a comparison of the display effect before and after removing the open circuit broken cross. You can see:

- The chip performs the function of removing the open circuit bad point cross, which can remove the bad point cross well and optimize the display effect.



Show the effect before removing the open break point cross

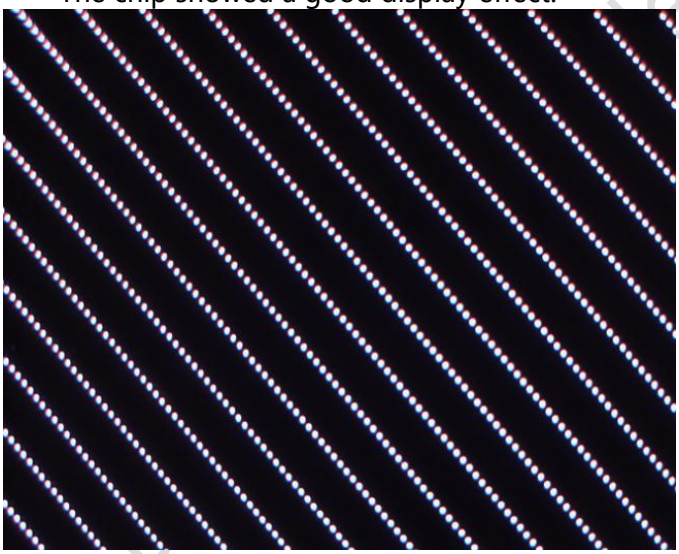


Show the effect after removing the open break point cross

10.1.2 Ghosting elimination and no banding effect

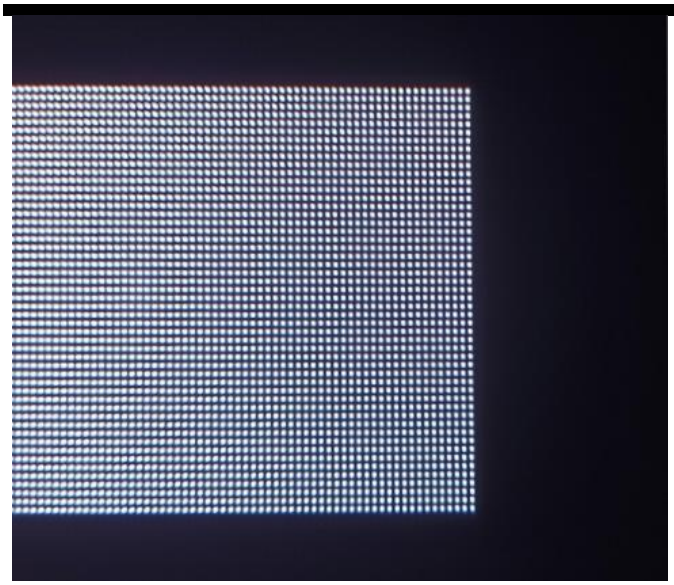
Here is the ghosting elimination and no banding effect, you can see:

- Inclined scanning ghost, text ghost and other problems can not be observed.
- Highlight block with bright, oblique scan superimposed highlight block with bright test shows very good results.
- The chip showed a good display effect.

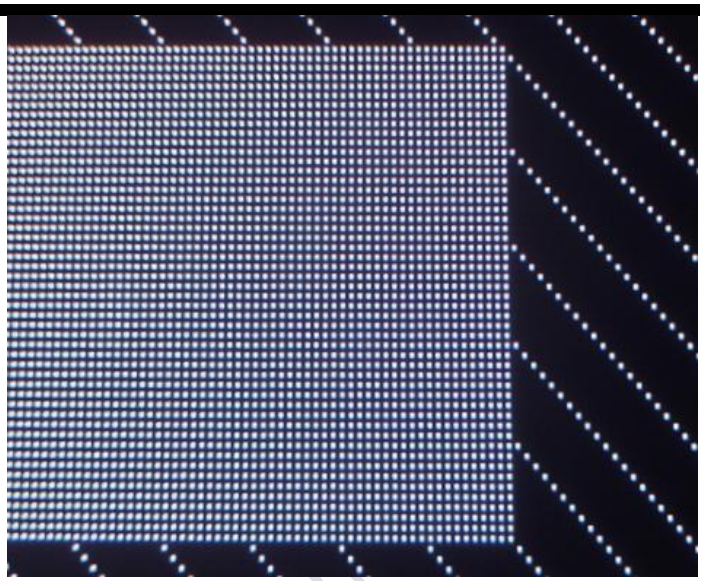


The oblique sweep ghost test showed the effect

Text ghost test shows the effect



The highlight block with the highlight test shows the effect

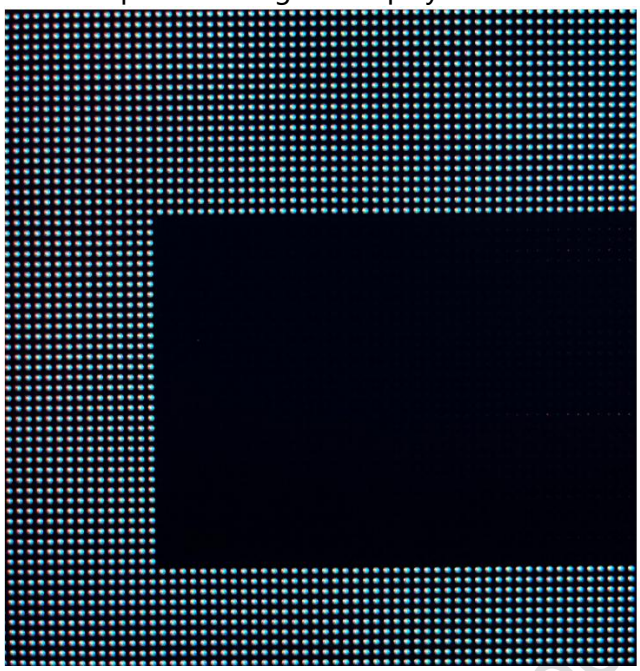


The oblique scan stack highlight block highlight test to show the effect

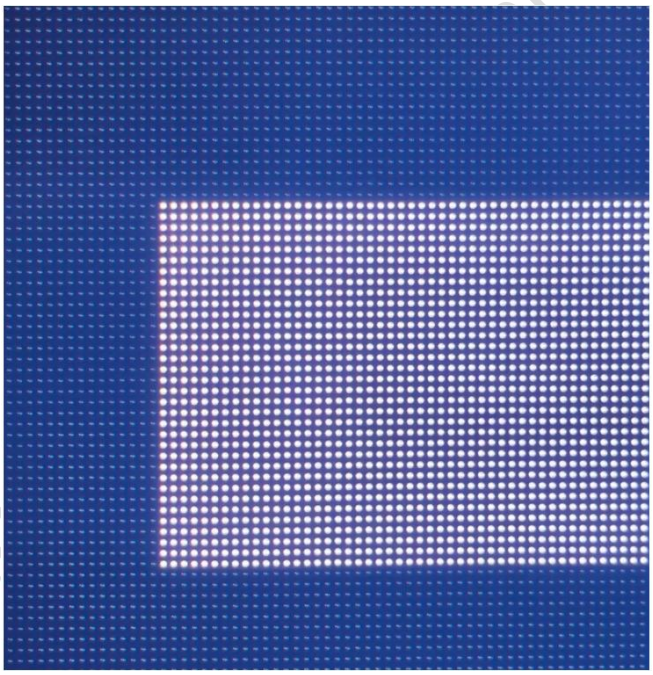
10.1.3 High and low ash interference and coupling, showing bad effect optimization

The following figure shows the optimization effect of high and low ash interference and coupling display. It can be seen that:

- Neither the low gray coupling between black block and white block can be felt.
- The chip showed a good display effect.



Black block low gray coupling test shows the effect



The white block low gray coupling test showed the effect

11 Instruction and registers

11.1 Register instructions

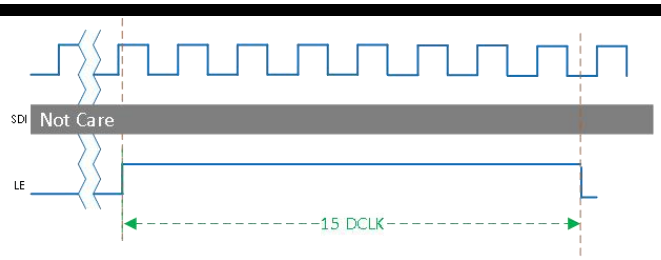
Directive name	LE	description
DATA_LATCH	1	Locch 16bit data to SRAM
VSYNC	3	Update the display data
WR_CFG	5	Write register
PRE_ACT	14	Write enablement
DDR	2	Enter double-along mode
SDR	≥15	Enter single-along mode

11.2 Data command

The order of data sent	Line	channel
1	Line 0	Channel 15 (OUT15)
2		Channel 14 (OUT14)
.....		.....
16		Channel 0 (OUT0)
17	Line 1	Channel 15 (OUT15)
18		Channel 14 (OUT14)
.....		.....
32		Channel 0 (OUT0)
.....		
1009	Line 63	Channel 15 (OUT15)
1010		Channel 14 (OUT14)
.....		.....
1024		Channel 0 (OUT0)

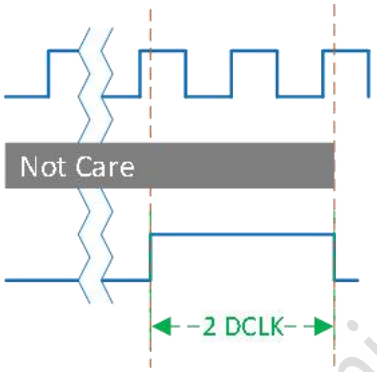
11.3 Singles and singles along the switch

1. The SDI data are sampled along the CLK rise in the single edge mode, and SDI data are sampled along both the rising and descending CLK in the double edge mode.
2. The OE signal width is fixed with the CLK ascending edge count
3. The odd-double edge mode switch instruction needs to be sent once.
4. If you need to power up into the single edge mode, you need to send the instructions shown in the following figure



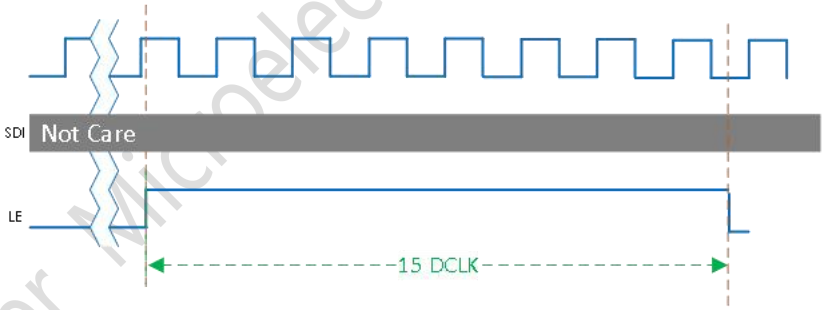
Greater than or equal to 15 DCLK edges (up + down) are set to SDR

If you need to power up and enter the double edge mode, you need to send the instructions shown in the figure below



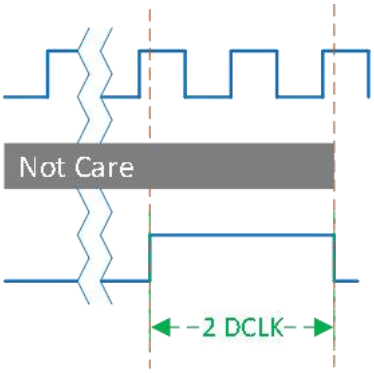
2 DCLK ascending edges were set to DDR

If you are already in double edge mode and need to enter single edge mode, send the instructions in the following figure



15 DCLK edges (up + down) is set to SDR

If you are already in the single edge mode, you need to enter the double edge mode



2 D CLK ascending edges in single edge mode are set to DDR

11.4 Write register

PRE _ ACT is sent first, then WR _ CFG is executed. LE is the width of 5 DCLK, the 8bit is the register address bit, and then the 8bit is the data bit of the corresponding register address.

for instance:

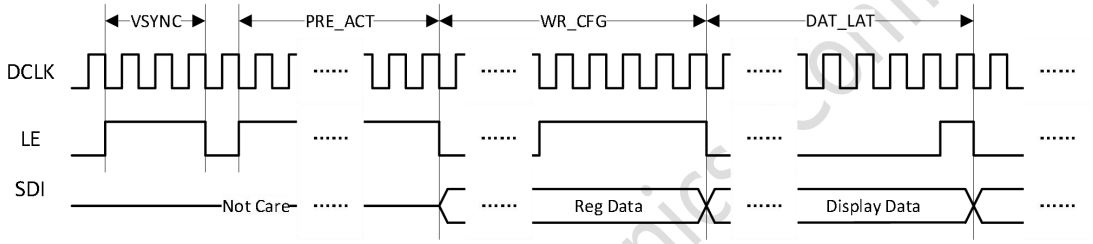
{A7, A6, A5, A4, A3, A2, A1, A0} = 8' b0000_0111;

{D7, D6, D5, D4, D3, D2, D1, D0}=8' b1001_1101;

That is, the register 0x07 (8 'b0000_0111) is set to 8' b1001_1101.

11.5 Sending mode of the register signal

The specific driving mode is as follows:



As shown in the figure above, the order of instructions and data in each frame:

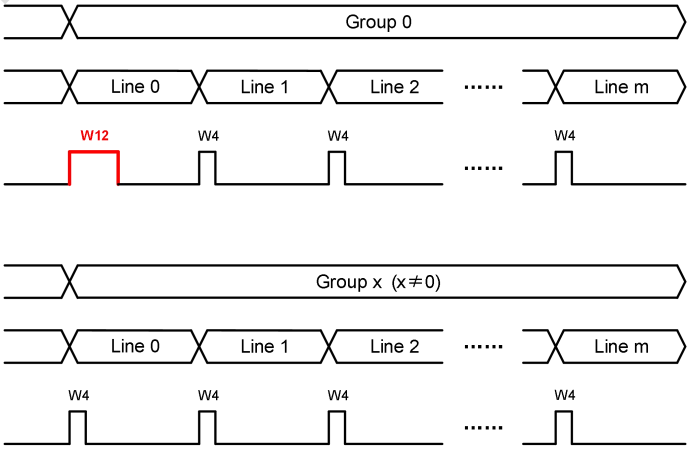
1. transmit by radio VSYNC.
2. Send the PRE _ ACT.
3. Send the WR _ CFG, and write to the register configuration. Each frame can write a register value of only one address to save configuration time.
4. Send DAT _ LAT several times and write the display data with SDI.

11.6 The ROW signal transmission mode

DP3369S The integrated GCLK generation circuit changes the OE signal of the universal constant current chip to ROW signal and uses ROW

The rising edge of represents the beginning of a row, where there are two types of ROW:

1. W12: The high level width representing ROW is the width of 12 DCLK
2. W4: The high level width representing ROW is the width of 4 DCLK

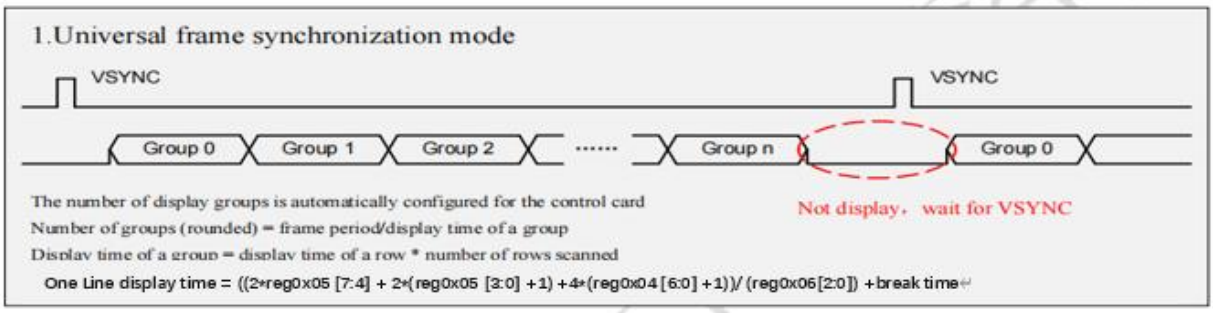


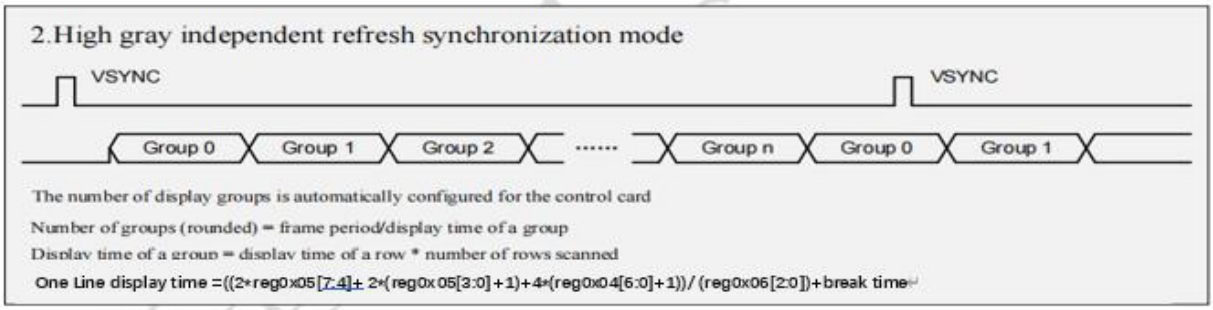
As shown in the figure above, when sending ROW signals, only the line 1 (Line 0) of group 1 (Group 0) needs to send W12 ROW signal, and other ROW signals are sent according to W4.

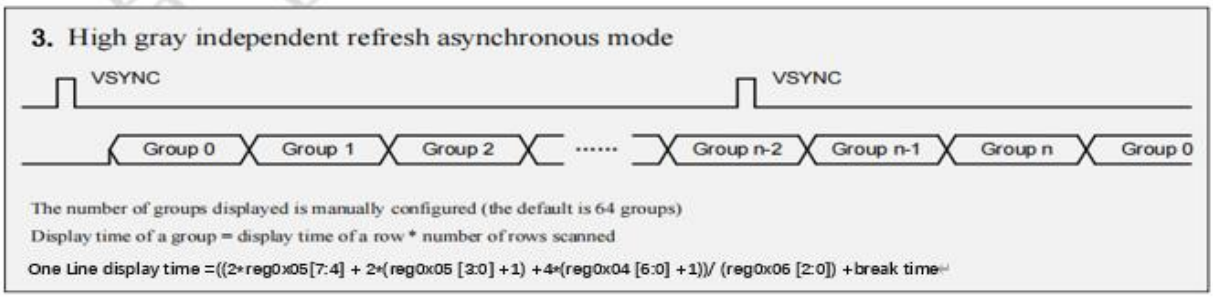
11.7 The PWM display mode

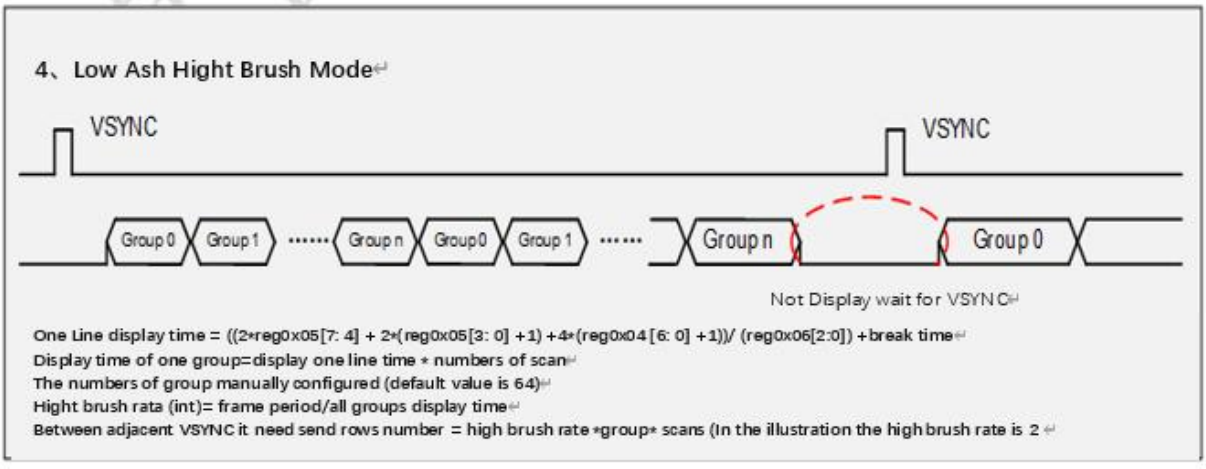
DP3369S Four PWM display modes are integrated in the tablet:

1. General frame synchronization mode; 2. Independent refresh synchronization mode of high ash data;
3. High ash data independently refresh the asynchronous mode; 4. Low ash and high brush mode









11.7.1 Universal frame synchronization mode

Working mode and related configuration are:

1. Set the PWM display mode to the universal frame synchronization mode
2. The number of DCLK in each line is calculated according to Eq
3. Configure the number of display data groups, reg0x03 [6:0] = refresh rate / frame rate-1
3. Line 1 (Line 0) of Group 1 (Group 0) is displayed after the VSYNC
4. Data display for the current frame is stopped until the arrival of the next VSYNC

11.7.2 High ash to independently refresh the synchronization mode

Working mode and related configuration are:

1. Set PWM display mode to high gray data independently refresh frame synchronization mode
2. Calculate a set of display time = frame period / (refresh rate / frame frequency)
3. Calculate the display time of a row = a set of display time / number of rows
4. The number of DCLK in each line is calculated according to the formula, which is satisfied by adjusting the line gray series and the DCLK frequency and the register reg0x6 [1:0]
5. ROW is sent continuously at a fixed display frequency. The frequency of ROW is independent of VSYNC, and the frequency of ROW signal = 1 / row of display time = 1 / time between two ROW rise edges
6. Group 0, Line 0, and W4, sends the ROW signal for W12, only one ROW signal, which continues in this way.

11.7.3 High ash to independently refresh the asynchronous mode

Working mode and related configuration are:

1. Set PWM display mode to refresh asynchronous mode with high gray data
2. The number of DCLK in each line was calculated according to Eq
3. The number of displayed data groups was manually configured by default to 64 groups (reg0x03 [6:0] =7'h3f) with a maximum support of 128 groups.
4. Frequency of the ROW signal = 1 / row of display time = 1 / time between two ROW rise edges
5. The number of groups to be displayed in a frame = display refresh rate / frame rate, and the number of groups to be displayed in a frame can be greater than the number of data groups configured in step 3. In this case, the control card needs to send (display refresh rate / frame rate * number of lines) ROW signals until the next vsync display is in the inter-frame black field state
6. Line 0 sends a ROW signal for W12, and a ROW signal for W4 for each (as configured by register value) * scanned) ROW signal, which continues in this manner.
7. The refresh rate can be greater than 7680

explain:

The main differences between the frame synchronization mode and the asynchronous mode are:

1. High ash data independent refresh frame synchronization mode: the number of display data groups is automatically configured according to the display frame time
2. High ash data independent refresh asynchronous mode: the number of data groups can be manually configured

11.7.4 High ash to independently refresh the asynchronous mode

Working mode and related configuration are:

1. Set the PWM display mode to low gray high brush mode
2. The number of display groups is manually configured (the default configuration is 64 groups)
3. The number of DCLK for each line is calculated according to the formula, and the display time of one row is calculated
4. Calculate a set of display time = one row display time * number of rows
5. Calculate all groups display time = one group display time * number of groups,
6. High brush rate (consolidation) = frame period / display time of all groups
7. Two Vsync need to send a high brush rate * display groups * scan a number of ROW signals
8. Line 1 (Line 0) of Group 1 (Group 0) is displayed after the VSYNC
9. The data for the current frame shows high brush times and stops the display until the arrival of the next VSYNC
10. Visual refresh rate = frame rate * number of data groups * high brush rate
11. The low gray and high brush mode only needs to change the ROW signal according to the above steps, and the gray level does not need to be adjusted

11.8 Relevant configuration as displayed by the PWM

11.8.1 Row scan number configuration

DP3369S Up to 64 row sweeps, configured as reg0x02 [5:0] = number of row scans-1

11.8.2 Line gray-scale series configuration

reg0x04 [6:0] represents the PWM display length of a row, and the PWM display length of a row is = 4 * (reg0x04 [6:0] + 1), with the maximum support of 128X4=512

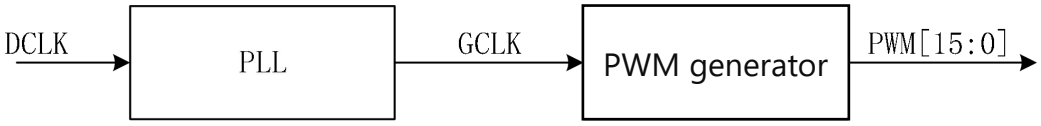
11.8.3 The PWM displays the grouping configuration

reg0x03 [6:0] shows groups for PWM, and groups for PWM = reg0x03 [6:0] + 1, and the maximum number of supported groups is 128 groups

In frame synchronization mode, PWM displays number of groups = refresh rate / frame rate

In asynchronous mode, PWM display groups can be configured independently (regardless of refresh rate)

11.8.4 Internal grayscale clock configuration



DP3369S PLL into the gray scale clock GCLK, the relevant calculation formula is as follows:

FGCLK = FDCLK * frequency division coefficient

11.8.5 PWM gray series as well as gamma generation

PWM gray series (maximum) = Line gray series * PWM display grouping

Gamma can be calculated and generated according to the PWM gray scale series (maximum value) (this part is generated by the control card manufacturer according to its own gamma generation formula)

The maximum chip gray series supports only 16bit

11.9 Open circuit detection and remove bad points

Check [remove bad points]: reg0x0c[1] =1;

Do not check [remove bad points]: reg0x0c[1] =0.

12 Packaging heat dissipation power (P_D)

The maximum heat dissipation power of the package body is determined by the formula $P_{D(\max)} = \frac{(T_j - T_a)}{R_{th(j-a)}}$

When all the 16 channels are opened, the actual power is:

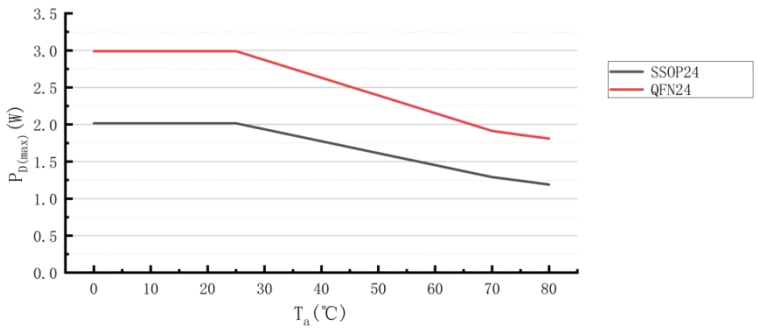
$$P_{D(act)} = I_{DD} * V_{DD} + I_{OUT} * Duty * V_{DS} * 16$$

To ensure that $P_{D(act)} \le P_{D(max)}$ The relationship between the maximum current and duty ratio is:

$$I_{OUT(\max)} = \frac{\frac{T_j - T_a}{R_{th(j-a)}} - (I_{DD} * V_{DD})}{V_{DS} * Duty * 16}$$

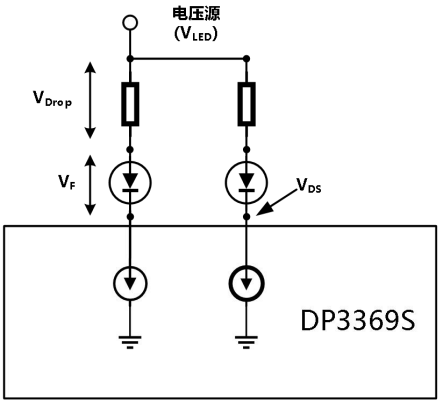
among T_j For the junction temperature (T_j=150℃) , T_a For the ambient temperature, and V_{DS} Is the constant current output port voltage, Duty is the duty cycle, $R_{th(j-a)}$ For the package of the thermal resistance.

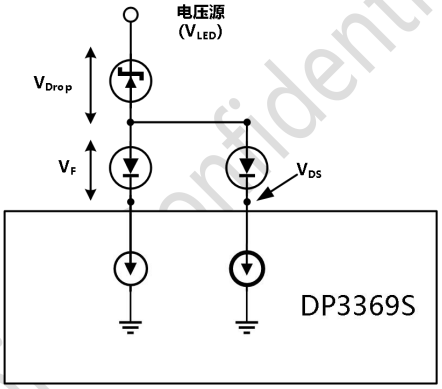
package	$R_{th(j-a)}$(℃/W)	$P_{D(max)}$(W)
QSOP24	62	2.01
QFN24	41.8	2.99



13 Load End Voltage (VLED)

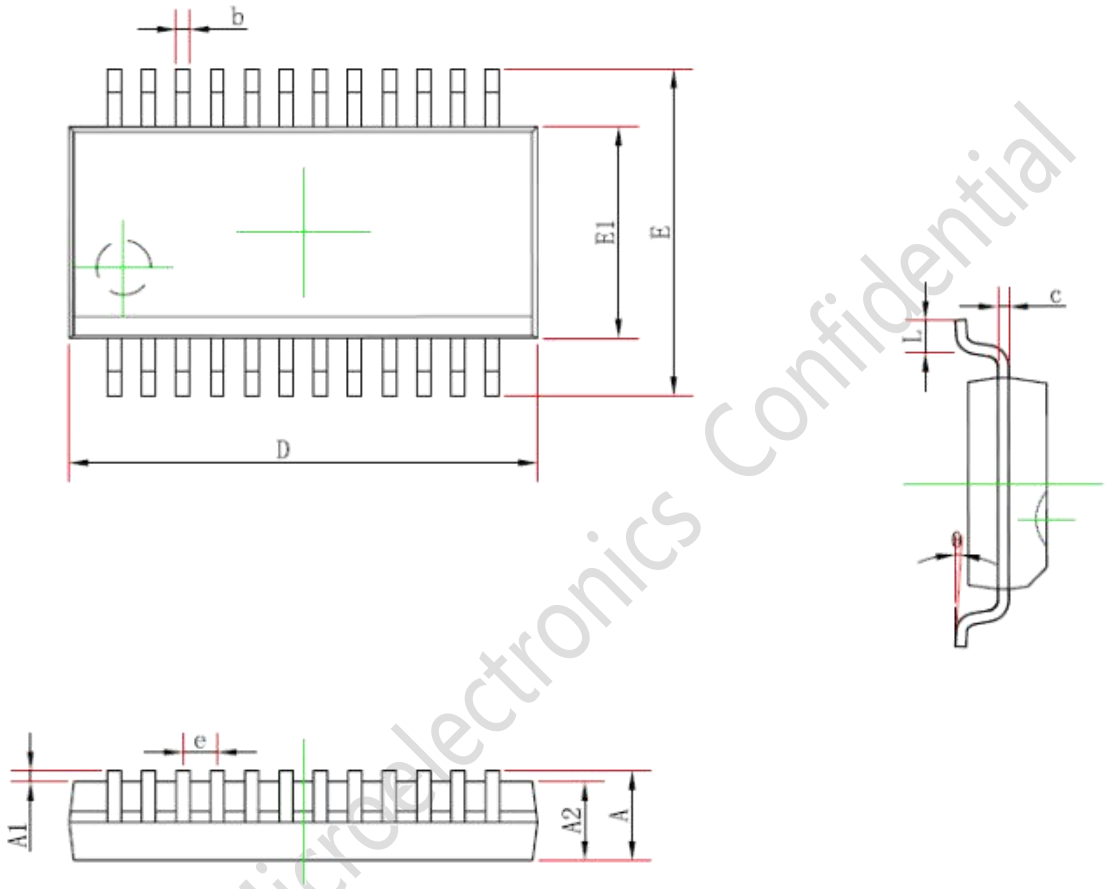
To optimize the heat dissipation capacity of the package, the output voltage (V_{DS}) The best operating range is 0.3V~1.0V (now I_{OUT}=0.5 ~ 36mA)。 if $V_{DS}=V_{LED}-V_F$a word used in a person's name V_{LED}=5V, when too high output voltage (V_{DS}) May result cause $P_{D(act)} > P_{D(max)}$; In this case, it is recommended to use a low V as low as possible$_{LED}$Voltage for use, can also be used as an external string resistance or voltage regulator tube as V_{DROP}. At the moment lead to $V_{DS}=(V_{LED}-V_F)-V_{DROP}$, To reduce the input voltage (V_{DS}) The effect of the value. The application diagram of the external string resistance or voltage regulator pipe can be referred to in the following figure.





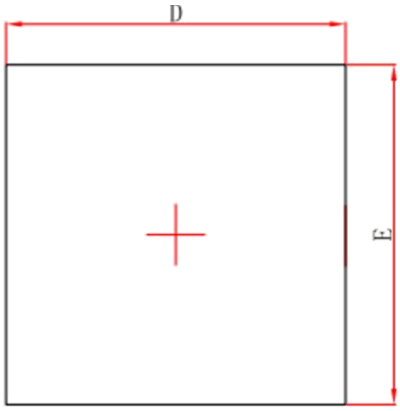
14 Packaging information

- QSOP24 Plastic sealing specification drawing

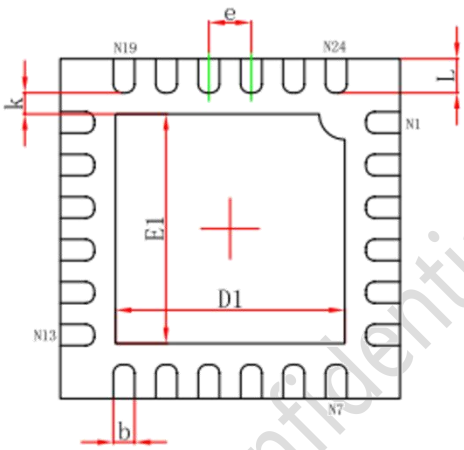


	millimetre (mm)	
	least value (Min)	crest value (Max)
A	—	1.95
A1	0.05	0.35
A2	1.05	—
b	0.1	0.4
c	0.05	0.254
D	8.2	9.2
E1	3.6	4.2
E	5.6	6.5
e	0.635TYP	
L	0.3	1.5
θ	0°	10°

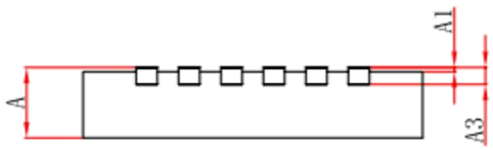
- QFN 24 plastic seal specification drawing



Top View



Bottom View



Side View

	millimetre (mm)	
	least value (Min)	crest value (Max)
A	0.700/0.800	0.800/0.900
A1	0.000	0.050
A3	0.203REF	
D	3.924	4.076
E	3.924	4.076
D1	2.6	2.8
E1	2.6	2.8
k	0.20MIN	
b	0.200	0.300
e	0.500TYP	
L	0.324	0.476

15 Official Announcement

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